IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Zhong Dong et al		
Assignee:	ProMOS Tech. Inc.		
Title:	METHOD OF FORMING ONO-TYPE SIDEWALL WITH REDUCED BIRD'S BEAK		
Serial No.:	10/821,100	Filing Date:	April 7, 2004
Examiner:	Vu David	Group Art Unit:	2818
Docket No.:	M-15295 US	Confirmation No.:	8965

San Jose, California
November 15, 2007

MAIL STOP Board of Appeals
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

A Notice of Appeal was filed 9/14/07.

A Pre-Appeal Conference Brief was simultaneously filed in response to the Final Office Action of July 13, 2007. The Pre-Appeal Conference Decision of 10/24/07 provided Applicant with a one month extension to file the present Appeal Brief.

The Appeal Brief fee required pursuant to 37 CFR §41.20(b)(2) is to be charged to the below identified and authorized Deposit Account.

Appeal Brief sections in compliance with 37 CFR §41.20(c)(1)(i)-(vii)-(ix) begin on page 2 of this paper.

LAW OFFICES OF
MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

(i) Identification of Real Party in Interest

The real party in interest is the Assignee of record: PROMOS TECHNOLOGIES INC. of HSING-CHU, TAIWAN (Reel/Frame: 015604/0267).

(ii) Related appeals and interferences

There are no other prior and/or pending appeals, interferences or judicial proceedings known to appellant, the appellant's legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(iii) Status of Claims

Claims 1-15, 21-23, and 24 were rejected under 35 USC §**103**(a) (as applied through §102(e)) as being obvious over **You** (US 6,706,613) in combination with **Wang** (US Pub 2005/0110102 published 5/26/05 on basis of an application filed 11/25/03). Reference was also made to **Fujimoto** (US 6,830,973) and to **Xing** (2003/0124873) as part of the justification for rejection.

Claims 11, 26 and 27 were rejected under 35 USC §**112** as lacking written description support. (No art was applied against claims 26-27.)

Claims 25 and 28 were indicated to contain allowable subject matter.

Claims 16-20 had been canceled.

All rejections are being appealed here, namely those pending against claims 1-15, 21-24, and 26-27 .

(iv) Status of Amendments

No amendment was filed subsequent to the final rejection of 7/13/2007. However arguments in response to the final rejections were filed 8/14/2007 and 9/14/2007 (the latter being the Pre-Appeal Conference Brief).

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

(v) Summary of Claimed Subject Matter (including reference to support in the filed application)

Independent **Claim 1** is directed to a method of forming sidewall dielectric [*350 of Fig. 3C, spec pg.24, ¶0060*] on an ONO-type memory cell stack [*110 of Fig. 1A, spec pg.9, ¶0035*] where at least one sidewall of the ONO-type memory cell stack includes at least three "exposed" [*Last sentence of ¶0035*] material layers [*112-115 of Fig. 1A, spec pg.13, ¶0042*] with at least two of the exposed material layers being respectively composed of an oxide [*114*] and an oxidizable material [*112*] disposed adjacent to the oxide, and where the method comprises: (a) subjecting the at least one sidewall to a "dry" ISSG process (In-Situ Steam Generation) where the "dry" ISSG [*320 of Fig. 3A, spec pgs.19-21, ¶0054-56*] process comprises: (a.1) flowing [*See pg.12, ¶0041 where "flow" of DCS is defined*] molecular oxygen (O2) towards the stack; and (a.2) flowing molecular hydrogen (H2) towards the stack, where the volumetric flow ratio of the H2 to the O2 is less than about 0.2 [*See last sentence of ¶0040 where "unstable" is defined and pg.20, ¶0054*].

Independent **Claim 23** is directed to a method of forming sidewall dielectric on an ONO-type memory cell stack where at least one sidewall of the ONO-type memory cell stack includes at least three exposed material layers with at least two of the exposed material layers being respectively composed of an oxide and an oxidizable material disposed adjacent to the oxide, and where the method comprises: (a) subjecting the at least three exposed material layers of the sidewall of the ONO-type memory cell stack to a dry ISSG process (In-Situ Steam Generation) where the dry ISSG process generates short lived oxygen radicals [*See pg.22, ¶0058 and 327a,b in Fig. 3A*] whose reactivity extinguishes before the short lived oxygen radicals are able to permeate laterally [*Pg.22, ¶0058 and see also 129a,b in Fig. 1B*] as deep into said exposed oxide material of the ONO-type memory cell stack and oxidize materials therein as would the reactive oxygen of a dichlorosilane-based High Temperature Oxidation (HTO) process [*Fig. 1B*] applied to an essentially same ONO-type memory cell stack [*110' in Fig. 1B*] .

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

(vi) Grounds of Rejection to be Reviewed on Appeal

6.1: (Finding of Fact): The final rejection of 7/13/2007 (hereafter also "FOA") at pg. 4, ¶2 alleges that You 613' teaches to directly oxidize the "*exposed*" material layers of You's ONO stack (Fig. 2B) with a thermal oxide process. An additional finding buried within this ground of rejection is that the ordinary artisan would reasonably see You's silicon nitride layer 106a as being an "*oxidizable*" part of the ONO-type structure (in the framework of solving the problem of reducing Bird's Beak).

6.2: (Finding of Fact): The final rejection of 7/13/2007 (FOA) at pgs. 7-8, ¶6 alleges that You 613' teaches "*dry oxidation*" (meaning, no hydrogen) merely as an example or one possible choice and that the person of ordinary skill would not see any element of You '613 as being critical or essential unless You had expressly said so. Therefore the FOA concludes that an ISSG process is obviously substitutable into the environment of You '613 for achieving more "*excellent thickness*" results and for improving on "*thermal budget*" (FOA pg. 5, line 1). The FOA references the Abstract of Wang for supporting its allegation regarding "excellent thickness".

6.3: (Review of Evidence): The FOA at pg. 8, end of ¶6 rules that Applicant's submitted Rule 132 Declaration (of Nov. 2006) "*merely states an opinion*" regarding what the ordinary artisan "would avoid" and that the Rule 132 Declaration "*reads too much*" into what the "dry oxidation" language of You '613 means to one of ordinary skill. The FOA at page 8, end of ¶6 then dismisses all the rest of Applicant's rebuttal evidence and rebuttal arguments by concluding: "*In all, the arguments are not persuasive*".

6.4: (Finding of Fact): The FOA at pg. 4, ¶2 alleges as fact that the only thing You 613' fails to teach beyond the taught direct oxidizing of the allegedly "*exposed*" material layers of You's ONO stack (Fig. 2B) with a thermal oxide process is the use of a specific "*dry*" ISSG process in place of You's oxygen-only oxidation process. The FOA concludes as a matter of fact that Wang '102 teaches to the ordinary artisan to try a wide range of ISSG processes for forming a sidewall, not only for the non-ONO structure of Wang Fig. 4E where lateral permeation of oxygen is not an issue, but also as an obvious variation for the ONO stack structure (120) of You Fig. 2A (where the latter contains a problematic metal-silicide layer 112 discussed below) under the rational that Wang teaches that its full range of

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

mentioned ISSG processes always **"provides excellent thickness control and the thermal budget can be reduced"** irrespective of the specific structure being oxidized. (See also FOA pg. 7, end of ¶5 where the Office action asserts that this stated basis for combining references is unrebutted "*common knowledge*" and therefore proper motivation.)

6.5: (Review of Evidence): The FOA of 7/13/07 does not address at least the following points of rebuttal evidence raised by the Rule 132 Declaration of record: **(a)** the ordinary artisan would understand that You's ONO stack layers are not "*exposed*" at the time of oxidation (Rule 132 ¶4k); **(b)** the ordinary artisan would be motivated to not use hydrogen in the presence of You's exposed metal silicide layer (Rule 132 ¶4m) and therefore the ordinary artisan would be guided away from combining You with Wang because You teaches away by calling for "*dry oxidation*" (Rule 132 ¶4d); **(c)** under the common sense of, if-it-isn't-broken, then-don't-fix-it, the ordinary artisan would resort to industry standard processes (HTO, dry oxidation) for forming sidewall because they are well understood in the industry. The ordinary artisan would not instead engage in expensive and undue new experimentations with exotic ISSG formulations (Rule 132 ¶4i); **(d)** the ordinary artisan would not see the rational of the FOA regarding "*reduced thermal budget*" because the dry ISSG process of the claims does not reliably produce a stable exothermic hydrogen flame at the sidewall surface (Rule 132 ¶4e); and **(e)** each prong of the two prong motivation supporting the §103 rejection ("provides *excellent thickness control* and the *thermal budget* can be reduced") is rebutted by the Rule 132 Declaration as being factually incorrect and thus the allegation in the FOA that the stated motivation is unrebutted "*common knowledge*" is itself factually incorrect.

6.6: (Review of Arguments): The post-final Advisory Action of 8/24/2007 does not address any of Applicant's post-final arguments as filed prior to Appeal, including that common sense would motivate the ordinary artisan to use the tried and proven, existing solutions for Bird's Beak, including You 613's approach of forming a protective nitride film coating and only thereafter using "dry" oxidation on the protectively coated sidewalls rather than trying something radically new and heretofore unproven as to effectiveness.

6.7: (Review of Arguments): Rejections for lack of adequate written description remain of record against Claims 11, 26, 27 (see FOA at pgs. 2-3, ¶1). The post-final Advisory Action of 8/24/2007 does not address any of Applicant's arguments filed prior to Appeal

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

regarding the §112 rejections, and thus Applicant is unsure of what the Examiner's current position is regarding Claims 11, 26 and 27.

6.8: (Miscellaneous): With regard to Claim 12, the FOA asserts contrary to 35 USC §100(a) that "discovery" (of optimal results) is not patentable. With regard to Claims 13-14, the FOA asserts that there is a specific ISSG process taught by You and Wang that inherently produces the claimed results. With regard to others of the dependent claims there have been no showings of the recited limitations as is detailed below.

(vii) Arguments

(The contentions of appellant with respect to *each* ground of rejection presented for review in paragraph (c)(1)(vi))

7.1 Agreement and Parting of Ways

Appellant and Examiner both agree that You '613 teaches a method for reducing Bird's Beak formation in an ONO stack where the Bird's Beak results from permeation of oxidizing agents.

You col. 2, lines 27-31 teach: "However, the oxidizing agents may permeate from the ~~upper portion~~ [sidewall lower edge] of the [poly & silicide] control gate 25 to[ward] the central portion B of the ONO layer 16 [of Fig. 1] so that a **bird's beak A** may occur as shown in FIG. 1".

> --Emphasis added. Strikeout and bracketed text added to fix an obvious translation error and to clarify that element 25 is comprised of poly layer 18 plus silicide layer 20. The oxidizing agents permeate inwardly towards the central vertical axis of the ONO stack. You's region A includes a lower edge portion of gate 25 (of poly 18) that has been consumed by oxidation and an upper edge portion of poly gate 14 that has been consumed by oxidation.

Appellant and Examiner part ways on the directions along which You '613 and Wang '102 send the ordinary artisan.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Appellant submitted a Rule 132 Declaration in November 2006 concomitant with the filing of a first RCE after the first Final Office Action of 06/06/2006. This appeal is taken from the second FOA of 7/13/2007 wherein the Rule 132 Declaration is dismissed as mere opinion.

The Rule 132 Declaration supports many of Appellant's below contentions. Established case law requires the PTO to demonstrate full consideration of all rebuttal evidence. However, to date, the PTO has failed to address all points raised in the Rule 132 Declaration. This is contrary to law. See In re Kumar 76 USPQ.2d 1048 (Fed. Cir. 2005) {"The *prima facie* case is a procedural tool, and requires that the examiner initially produce evidence sufficient to support a ruling of obviousness; thereafter the burden shifts to the applicant to come forward with evidence or argument in rebuttal. Piasecki, 745 F.2d at 1475. **When rebuttal evidence is provided, the *prima facie* case dissolves, and the decision is made on the entirety of the evidence.** Oetiker, 977 F.2d at 1445; In re Spada, 911 F.2d 705, 708 (Fed. Cir. 1990); In re Rinehart, 531 F.2d 1048, 1052 (CCPA 1976). "} [Bolding added.] See also In re Alton 37 U.S.P.Q.2d 1578, 1582-1584 (Fed. Cir. 1996) {"[The] Examiner's final rejection ... contained **two errors: (1)** ... and **(2) the summary dismissal of the [expert's] declaration**, without an adequate explanation of why the declaration failed to rebut the [rejection]"}.

Moreover, there is no way to determine what "subject matter as a whole *would have* been obvious *at the time the invention* was made to a *person having ordinary skill in the art*" (35 USC §103) except by qualified opinion of a knowledgeable declarant regarding how the PHOSITA of §103 "would have" behaved because the PHOSITA of §103 exists only in the past as a legally hypothesized person. See for example, In re Sullivan, 84 USPQ.2d 1034, (Fed. Cir. August 29, 2007) {"The Board [committed legal error in that it] failed to consider each of these [three] declarations. ... [T]he Board **must** give the declarations *meaningful* consideration before arriving at its conclusion. Moreover, the Board was mistaken to assert that the declarations only relate to the use of the claimed composition. The declarations do more than that; they purport to show ... how the prior art taught away from the composition, and how a long-felt need existed for a new antivenom composition. ... [T]he claimed composition was not known, and whether it would have been obvious [to PHOSITA] depends upon consideration of the rebuttal evidence. Had the Board considered or reviewed the

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

declarations in any meaningful way, it might have arrived at a different conclusion than it did." [Bracketed text and emphasis added. Ellipses indicated skipped text.]}.

It is Appellant's contention that the PTO has failed thus far to give the filed Rule 132 Declaration meaningful consideration.

It is Appellant's contention that You '613 directs the ordinary artisan to always coat the sidewalls of an ONO stack with a silicon nitride film (one having strong Si-N bonds) prior to formation of sidewall oxide so that lateral permeation of oxygen into the stack via lateral oxide pathways will be retarded by the silicon nitride skin. **This teaching guides away from the claimed invention.** You '613 pre-conditions the sidewall of "all" embodiments with nitrogen (see You col. 3, line 10). The Rule 132 Declaration of record supports this contention.

It is Appellant's contention that You '613 directs the ordinary artisan to only use a "dry" oxidation, which in the context of You means no hydrogen, and that this teaches away from combining with the hydrogen-based processes such as that of Wang '102. The Rule 132 Declaration of record supports this contention.

Appellant and Examiner both agree that Wang '102 teaches a method for reducing an oxidation thickness difference observed when conventional "*wet oxidation*" is applied to an open silicon surface and an adjacent nitride region (432 and 426 in Fig. 4E of Wang, see also 232 and 226 of Fig. 2E).

Wang pg. 1, paragraph [0005] states: "However, the oxidation selectivity of wet oxidation for the substrate and the silicon nitride layer is relatively high, that is, the oxidation rate of *wet oxidation* for the substrate is far greater than that of the silicon nitride layer." [Emphasis added.]

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Wang does not compare his ISSG processes against "dry" oxidation, only against "wet" oxidation. The purpose of Wang, as stated in his Abstract, is to "significantly reduce[ ] the processing time" for oxidizing the exposed "upper surface and the sidewalls of the silicon nitride layer" (426). This is done by maximizing the concentration of generated oxygen radicals. According to Wang paragraph [0032]: "The oxygen radical **peak** *concentration* results from a balance of radical generation through molecular collisions that are strong functions of temperature and pressure, and recombination processes ... the ISSG process depends upon using process pressure, flow rate and temperature in the chamber within specified ranges. Accordingly, in some embodiments the following parameters can be effective" [emphasis added].

It is Appellant's contention that the word "*some*" in the above last line means not all. The Rule 132 Declaration of record supports this contention. The Rule 132 Declaration of record supports this contention. (See Rule 132 ¶5d.)

It is Appellant's contention that the phrase "*within specified ranges*" means those that result in an "oxygen radical peak concentration" because that is the way that Wang minimizes time for oxidation. He generates as many oxygen radicals as possible for thereby maximizing reaction rates and minimizing time needed for oxidation to a desired thickness. Wang does not teach or remotely suggest the concept of *shortening* oxygen radical lifetimes by supplying a flow of hydrogen that is insufficient to sustain a stable hydrogen flame. The thrust of Wang's teachings are to maximize rather than shorten the lifetimes of ISSG-generated oxygen radicals. This is done so that, per Wang paragraph [0006], "Then the [peaked concentration of] reactive oxygen radical can effectively oxidize the silicon or silicon nitride on the substrate" [bracketed text added]. Note Rule 132 ¶5d where it is explained that Xing '873 guides artisans to lengthen radical lifetimes.

It is Appellant's contention that the FOA uses Applicant's disclosure as a blueprint for picking and choosing by hindsight (e.g., by ignoring Wang's main thrust regarding the maximizing of oxygen radical concentration) only that which supports a preordained conclusion of obviousness. See ¶5h of the Rule 132 Declaration which states: "It seems to me that the Patent Office is copying the idea of using dry ISSG for Birds' Beak out of the subject patent application and then projecting it by way of hindsight into Wang '102 at the portion of

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

OA page 3 where they mention Xing '873 as evidence of the state of the art." [Emphasis added.]

Appellant and Examiner both agree that Wang '102 recites a wide range of ISSG process parameters: "[0018] In some embodiments ... the H_2 and O_2 are introduced at flow rates proportionately in a range (H_2/H_2+O_2) about 0.1% to about 40%, **more usually** in a range about 5% to about 33% (H_2/H_2+O_2), and in particular embodiments at flow rates proportionately about 1:19 or 1:3 or 1:2 ..." [Emphasis added.]

Appellant and Examiner part ways however on the understandings that the ordinary artisan would draw from this text (e.g., the "**more usually**" language); particularly as it regards the unusual, relatively "dry" low end of the broad range in the "about 0.1% to" about 5% range. (It should be noted that the ratio expressed as (H_2/H_2+O_2) is not the same as the ratio expressed as (H_2/O_2). For example when quantities of H_2 and O_2 are equal, the first ratio equals 1/2 while the second ratio equals 1/1. The You reference speaks in terms of the first ratio while Appellant's claims speaks in terms of the second ratio. Appellant does not agree with the voodoo math used by the FOA at page 4 thereof. The Rule 132 Declaration at end of paragraph 5L explains that the correct conversion is that an H_2/O_2 ratio of x becomes an $H_2/(O_2 + H_2)$ ratio of $x/(1+x)$ so that, as x approaches unity, the value of $x/(1+x)$ approaches 50%.)

The Examiner, if understood correctly, appears to have made a finding of fact that the ordinary artisan would see Wang as teaching that ISSG always provides "*excellent thickness control*" (which phrase, by the way, is not in Wang's disclosure) and "*reduced thermal budget*" no matter what value of (H_2/H_2+O_2) is used in the broadly recited outer range (about 0.1% to about 40%) and no matter what the details are of the structure being subjected to any specific ISSG within this broad range.

By contrast, it is Appellant's contention that the ordinary artisan would treat the unusual and relatively "dry" low end of the broad ISSG range recited in the patent publication

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

document with great skepticism and as being problematic because it cannot support a stable hydrogen flame and it therefore does not maximize concentration of oxygen radicals per Wang's teachings. Moreover, an unstable flame fails to reduce thermal budget because thermal budget is instead reduced by stable ISSG wherein the exothermic heat of a lit and maintained hydrogen flame provides a localized temperature boost to the surface at which the stable flame is present. See ¶4e of the Rule 132 Declaration ("... the hydrogen flame provides localized exothermic heat, and without the flame, a non-local source of heat will probably have to be used (i.e., Rapid Thermal Heating lamps) and this will tend to hurt rather than help the thermal budget of the overall chip. ... As I already explained above, ISSG cannot be arbitrarily used in every arbitrary situation. If a metal silicide is present for example, the ordinary artisan should be highly motivated to not use an oxidation process that exposes the silicide to hydrogen. The ONO stack structure of You '613 constitutes such a situation. Thus, the ordinary artisan would have no motivation for combining You '613 and Wang '102." [emphasis added]).

It is Appellant's further contention that the ordinary artisan would not see Wang '102 as suggesting that lateral permeation of oxygen through oxide pathways of an ONO stack can be reduced by specifically using the relatively "dry" end of the broadly recited ISSG range.

Comparison of Wang Figs. 2E and 4E shows that Wang teaches in 4E to not have a completed ONO stack at the time ISSG is performed. Fig. 2E has an oxide covered nitride layer 226 while Fig. 4E teaches that the nitride layer 426 should have its upper surface open at the time ISSG is applied. Then in Fig. 4F ones sees the result, including the large oxide bulge 434 formed over silicon area 432.

It is Appellant's further contention that the ordinary artisan would see **Wang as teaching that ISSG produces significant Bird's Beak because Fig. 6 of Wang explicitly shows a large Bird's Beak structure (634)** being formed as a result of ISSG. This structure 634 corresponds to bulge 434 of Fig. 4F. See ¶5h of the Rule 132 Declaration ("... Bulging oxide growth 434 indicates volume enlargement as silicon implant region 432 and substrate are thermally oxidized. Wang provides no suggestion that a relatively dry ISSG might reduce lateral advancement of an oxidation front due to reduced lifespan of oxygen radicals ..." [emphasis added]).

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

The FOA of 7/13/2007 asks the reviewers to erase from their sight the **large Bird's Beak structure (634)** that is shown to be formed as a result of ISSG in accordance with Wang.

The FOA of 7/13/2007 asks the reviewers to pretend that the ordinary artisan would not see the bulging Bird's Beak structure 634 of Fig. 6 or the bulging oxide counterpart 434 in Wang Fig. 4F.

This is a picking and choosing is the hallmark of hindsight and is contrary to law. The ordinary artisan (PHOSITA of §103) would have seen the bulges and would have concluded from these that Wang's ISSG processes are not useful for reducing Bird's Beak and would have been guided away from combining Wang with You at least for this reason if not also for the facts that You teaches a completely different mechanism based on a nitride barrier and You calls for a metal silicide layer 20 within his composite control gate 25 (of Fig. 1, see also 111 and 109 of Fig. 2A).

7.2 Errors in construction of Claims 1, 23 and/or Erroneous Findings of Facts

Proper rejection is predicated on proper claim construction and on proper reading of the prior art.

Claims 1 and 23 contain the word "exposed". At this juncture it is unclear to Appellant/Applicant whether the outstanding grounds of rejection (FOA of 7/13/2007) interpret the word "exposed" to mean not-exposed or whether the outstanding grounds of rejection interpret You col. 6, lines 25-37 as not calling for the singular "a film containing nitride" that coats the stack sidewall 120a prior to oxidation. As such, Appellant/Applicant contingently assumes each in the alternative and argues that either the word "exposed", as it appears in Claims 1 and 23 is not being properly construed or that the nitride containing single coating film of You '613 is not being properly accounted for.

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Regrettably, the outstanding grounds of rejection do not address You col. 6, lines 25-37 where You explicitly teaches that the sidewall 120a of ONO stack 120 (Fig. 2B) is not exposed, but that it is instead covered with **"a film containing nitride"** and that this nitride

containing coating resists breakdown "so that oxidizing agents do not appear to penetrate [through the coating and] into the central portion of the ONO layer 108." [Bracketed text added.]

The Rule 132 Declaration of Nov. 2006 does address You col. 6, lines 25-37 and finds at ¶4k thereof that:

> [I]t would have been very clear to an artisan of ordinary skill that You '613 teaches at col. 6, lines 8-37 to use silicon nitride as a thin diffusion barrier on the sidewall of an ONO stack for precisely this purpose; for slowing down lateral permeation of oxygen into the interior of the stack during thermal oxidation of the sidewalls of his FG/ONO/CG stack 120 of Fig. 2B. You '613 implicitly teaches at col. 6, lines 36-37 that, were it not for the S-N (*sic*) bonds formed in his nitrogen pre-anneal step of col. 6, lines 8-25, that "oxidizing agents" would have "penetrate[d] into the central portion of the ONO layer 108 [in other words, deep into region "A" of You Fig. 1, reaching as far as the outer boundary of region "B"]" [*Bracketed text added*]. You '613 unequivocally teaches at col. 6, lines 29-35 that a film containing strong silicon-nitrogen bonds (S-N bonds) (*sic*) should be formed on the sidewall 102a of stack 120 before the stack is subjected to the thermal oxidation (to the "dry oxidation" of col. 6, lines 38-40). The pre-oxidation anneal in the nitrogen containing atmosphere causes the sidewalls in You's stacked gate structure 120 to be covered and protected by a thin nitride film such that they are not directly exposed to the thermal oxidation environment. In other words, You's stacked gate structure 120 does not have openly exposed oxide to serve as a gateway through which oxygen can readily enter laterally into the interior of the ONO structure to thereby quickly begin the process of Bird's Beak intrusion. You's ONO structure is covered on its sidewall with nitride before thermal "dry oxidation" is initiated at col. 6, lines 38-40. This aspect of You '613 is not ambiguous or open to reasonable debate. Instead, it is the whole basis of the invention described by You '613. You uses the thin nitride coating to slow down entry of laterally permeating oxygen into the regions between his FG and CG layers, and to thereby reduce the Bird's Beak incursion as is shown in region "C" of You Fig. 2C.

When placed on opposed sides of a scale that measures preponderance of evidence, the silence by the outstanding FOA regarding You col. 6, lines 25-37 is outweighed by the Rule 132 Declaration irrespective of how little credibility is attributed to the Rule 132 Declarant because something always outweighs nothingness. (Additionally, the PTO has produced no showing to challenge the credibility of the Rule 132 Declarant.)

In contrast to the nitride coated ONO stack of You '613 (as established at least by the above quoted portion of ¶4k of the Rule 132 Declaration), the preamble of rejected Claim 1 calls for "an ONO-type memory cell stack where at least one sidewall of the ONO-type memory cell stack includes at least three exposed material layers with at least two of the

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

exposed material layers being respectively composed of an oxide and an oxidizable material disposed adjacent to the oxide" [emphasis added].

The body of Claim 1 makes antecedent reference to the preamble (to "the at least one sidewall"). The final rejection of 7/13/2007 (FOA) at pg. 4, ¶2 does not dispute that the preamble is due patentable weight and instead apparently finds either as claim construction that exposed means not exposed; or finds as fact that You 613' teaches to directly oxidize the allegedly "exposed" material layers of You's ONO stack (Fig. 2B) with a thermal oxide process ("for example a dry oxidation" per col. 6, line 39 of You). Interestingly, as part of this ground of rejection against Claim 1, the FOA goes out of its way to find that You's silicon nitride layer 106a is the primary equivalent to the "oxidizable material disposed adjacent to the oxide" as recited in Claim 1. The pre-RCE first FOA of 06/06/2006 did not identify an equivalent in You for the "oxidizable material".

7.3 Selective Picking and Choosing

An essential part of the §103 rejections against Claims 1 and 23 is the allegation (at FOA pg. 5, line 1) that the person of ordinary skill would view Wang's ISSG processes as always providing "**excellent thickness control and the thermal budget can be reduced**". Appellant demonstrates herein that each prong of this two-pronged basis is without basis.

With regard to the alleged "*excellent thickness control*" aspect, it is to be observed that Wang does not compare ISSG against dry oxidation with O_2 but rather against "wet oxidation". (See again Wang pg. 1, paragraph [0005] as partially reproduced above.) Moreover, Wang never uses the phrase, "*excellent thickness control*". That is something fabricated out of thin air by the FOA. Instead Wang states: "[0016] In some embodiments the ratio of the thicknesses of the resulting second silicon oxide layer and gate oxide layer is in the range about 0.6:1 to about 0.8:1." [Emphasis added.]

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
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With regard to the alleged reduction of "*thermal budget*" aspect, it is to be again observed that Wang does not compare ISSG against dry oxidation with O_2 but rather against "wet oxidation". At paragraph [0003] Wang sates: "[I]n conventional processes[,] oxidation of

silicon nitride is time-consuming and has a very high thermal budget. In some conventional processes, for example, silicon nitride is oxidized by wet oxidation within a furnace at a temperature of 1000°C over a time period as long as 60 minutes."

In view of the above, there is no factual basis for asserting that the ordinary artisan would view any of Wang's ISSG processes as promising a reasonable likelihood of either "*excellent thickness control*" as compared to dry oxidation with O_2 or reduction of "*thermal budget*" as compared to dry oxidation with O_2. Yet these are the only motivations by way of which the FOA justifies the combining of Wang with You. These are the only motivations by way of which the FOA justifies the replacement of You's dry oxidation with only O_2 (after a silicon nitride film has been grown) with an ISSG process cherry picked out of the extreme lower, dry end of Wang's broadly recited outer range "(about 0.1% to about 40%)". Incidentally, 40% in Wang's terms becomes 66.7% in terms of the (H2/O2) ratio. (Let 40% equal x/(1+x) and then solve for x.) Nowhere does either of You or Wang promise that an ISSG of any arbitrary parameter will always provide "*excellent thickness control*" or reduction of "*thermal budget*" in the context of You's nitride coated ONO stack.

What we have here is a long string of selective omissions and additions by the FOA in its stretched attempt to reach the preordained conclusion of obviousness. The FOA appears to conveniently strip off from the ONO stack, the essential nitride coat required by the teachings of You '613. The FOA appears to conveniently strip out from You '613 the presence of the metal silicide layer in the ONO stack. The FOA appears to conveniently strip out from Wang '102 the Bird's Beak features 634 that are so prominent in Fig. 6. The FOA appears to conveniently add into Wang a teaching that is simply not there, namely that an ISSG of any arbitrary parameter will always provide "*excellent thickness control*" and reduction of "*thermal budget*" in the context of You's ONO stack and relative to any other method of oxidation. (Wang compares his ISSG only against "wet" oxidation and only with respect to his non-ONO structure of Fig. 4E.).

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

It is well established that such serial pickings and choosings are impermissible. See for example, In re Hedges 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986) "[T]he prior art as a whole must be considered. The teachings are to be viewed as they would have been viewed by one of ordinary skill. ... It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art."

The person of ordinary skill as defined in 35 USC §103 cannot ignore Wang's oxide bulge 434 and its exposed predecessor 432 in Fig. 4E. It is to be kept in mind that You's stated goal is to avoid formation of such structural deformations (see You col. 2, lines 27-41) by first pre-conditioning "all" embodiments with nitrogen (see You col. 3, line 10). Wang by contrast has the open silicon region 432 in Fig. 4E. Thus You and Wang teach away from one another.

There is no evidence that Wang's ISSG processes would be effective in combination with You's stack where the latter contains a metal silicide (112 of You Fig. 2B, col. 5, line 20). There is evidence to the contrary, namely, that presence of hydrogen will present a problem for the metal silicide layer.

The person of ordinary skill would readily recognize that there is no ONO stack in Wang Fig. 4E, let alone one comprising a metal silicide layer. The person of ordinary skill would readily recognize that bulge 434 of Wang's post-oxidation Fig. 4F corresponds to the Bird's Beak analog shown as 634 in Wang Fig. 6. Note that 632 of Fig. 6 corresponds to 432 of Fig. 4F; 627 of Fig. 6 (the fully encased nitride) corresponds to 427 of Fig. 4F (the fully encased nitride) and 638 of Fig. 6 corresponds to 4387 of Fig. 4G. Wang does not suggest that a specific dry form of ISSG should be tried for purpose of reducing Bird's Beak formation in an ONO stack and neither does You '613.

Appellant's position regarding Wang is supported by ¶5h of the Rule 132 Declaration which states: "Bulging oxide growth 434 indicates volume enlargement as silicon implant region 432 and substrate are thermally oxidized. Wang provides no suggestion that a relatively dry ISSG might reduce lateral advancement of an oxidation front due to reduced lifespan of oxygen radicals and that this may in turn provide a useful solution to the long known and not fully solved, Bird's Beak problem. It seems to me that the Patent Office is

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

copying the idea of using dry ISSG for Birds' Beak out of the subject patent application and then projecting it by way of hindsight into Wang '102 at the portion of OA page 3 where they mention Xing '873 as evidence of the state of the art."

Appellant's position regarding the metal silicide layer (112) in You's stack is supported by ¶¶ 4c-4d of the Rule 132 Declaration which explain: "There is a very good reason for why You '613 insists on a "dry" oxidation. It is not a user-bypassable option. Hydrogen tends to act as a catalyst for encouraging decomposition of metal silicides." The Rule 132 Declaration concludes in this regard that: "because an ISSG atmosphere includes hydrogen, the ordinary artisan would see You '613 as teaching away from use of ISSG."

With regard to You '613, it should remain undisputed that col. 6, lines 25-37 teach: "These bonds of Si--N do not appear to break during the successive oxidation process so that oxidizing agents do not appear to penetrate into the central portion of the ONO layer 108" [emphasis added]. In other words, the oxidation process happens, successively, only after the protective nitride barrier is formed.

The FOA of 7/13/2007 appears to disagree with Applicant's contention that the "successive oxidation process" takes place only after the singular, "a film containing nitrogen" has been first formed on the exposed ONO stack so as to thereby cause the sidewalls of You's ONO stack to all become unexposed. The FOA instead makes reference at pg. 4 ¶2 thereof to a post-anneal process described at You col. 7, lines 58-67 which leaves "a silicon oxynitride film ... formed at the outer surfaces of the oxide film 116 [Fig. 2C] ... as was already described." [Bracketed text and emphasis added.] It is not understood how this reference to the supplemental SiON film aids the Examiner's case. The relied on text does not negate the fact that You col. 7, lines 23-35 still directs the ordinary artisan to use a nitrogen pre-treatment "so that the growth of an oxide film is at least partially restrained" and they still teach that the pre-oxidation exposure to nitrogen is responsible for "the substrate 100 is not significantly exposed to oxygen during the steps of loading and heating the substrate 100, the growth of a significant bird's beak can be restrained at the lateral portion of the ONO layer 108 during a successive oxidation process." [Emphasis added.] This is just another way of

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

saying that the protective nitride film is grown first and only afterwards, is the "successive" dry oxidation process pursued.

The issue in presenting a proper §103 rejection should not be one of picking and choosing convenient snippets of text from You '613, convenient snippets of text from Wang '102; but rather that of reading the whole of You for what it fairly teaches to one of ordinary skill without aid of hindsight and reading the whole of Wang for what it fairly teaches to one of ordinary skill without aid of hindsight.

To this end Applicant has submitted expert testimony regarding what the words and diagrams of You '613 would have meant to one of ordinary skill (to PHOSITA of §103) at the relevant time. At ¶4k of the Rule 132 Declaration, it is submitted that "[P]rior to the critical date, it would have been very clear to an artisan of ordinary skill that You '613 teaches at col. 6, lines 8-37 to use silicon nitride as a thin diffusion barrier on the sidewall of an ONO stack for precisely this purpose; for slowing down lateral permeation of oxygen into the interior of the stack during thermal oxidation of the sidewalls of his FG/ONO/CG stack 120 of Fig. 2B." Moreover it is found in the rebuttal testimony at the same ¶4k that "The pre-oxidation anneal in the nitrogen containing atmosphere causes the sidewalls in You's stacked gate structure 120 to be covered and protected by a thin nitride film such that they are **not directly exposed** to the thermal oxidation environment. In other words, You's stacked gate structure 120 does not have openly exposed oxide to serve as a gateway through which oxygen can readily enter laterally into the interior of the ONO structure to thereby quickly begin the process of Bird's Beak intrusion. You's ONO structure is covered on its sidewall with nitride before thermal "dry oxidation" is initiated at col. 6, lines 38-40. This aspect of You '613 is not ambiguous or open to reasonable debate. Instead, it is the whole basis of the invention described by You '613." [Emphasis added.]

7.3 Dependent Claims

With regard to Claim 3, the recited volumetric flow ratio of H2/O2 equal to, or less than, about 0.02 clearly falls below the usual 5% or more of Wang. additionally there is no showing that Wang defines parameters in terms of volumetric flow.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

With regard to Claim 4 there is no showing of rapidly heating the flowing gases as they flow towards said at least one sidewall.

With regard to Claim 5, there is no showing of the recited duration of about 20 seconds to about 300 seconds.

With regard to Claim 6, there is no showing of varying the O2 flow rate.

With regard to Claim 7, there is no showing of varying the H2 flow rate.

With regard to Claim 8, there is no showing of the specific chamber pressure in combination with the recited ratio of Claim 3.

With regard to Claim 9, there is no showing of the at least three *exposed* material layers.

With regard to Claim 11, there is no showing of the recited second silicon nitride layer. Additionally, Fig. 3A of the filed application does show an ONO stack that lacks a metal silicide layer.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

If understood correctly , the FOA appears to take the position with regard to method Claim 11 ("and further wherein: said ONO-type memory cell stack does not include a metal silicide layer" [*Emphasis added*]) that the written description of every patent regarding a method involving a chemical process taking place in a physical environment (that of the claim-defined, "ONO-type memory cell stack") must provide an explicit listing of all things that are excluded during the carrying out of the chemical process. In other words, rather than positively showing what the ONO-type memory cell stack does include as is done in Fig. 3A, the FOA position is that patent law requires Applicant to explicitly list all the things it does not include. No support is provided for such a legal proposition.

Drawings are part of the written description per Cooper Cameron Corp. v. Kvaerner Oilfield Prods., 291 F.3d 1317, 62 USPQ.2d 1846 (Fed. Cir. 2002) {"In *Vas-Cath*, we held that "under proper circumstances, drawings alone may provide a 'written description' of an invention as required by § 112." 935 F.2d at 1565, 19 USPQ2d at 1118. Drawings constitute an adequate description if they describe what is claimed and convey to those of skill in the art that the patentee actually invented what is claimed."}.

The FOA position is that; if an exclusionary list is not provided, Applicant is precluded from noting in the claim that the illustrated ONO-type memory cell stack does not include a metal silicide layer even though it is an indisputable fact that the illustrated ONO-type memory cell stack in Fig. 3A does not include a metal silicide layer and a person of ordinary skill would see this to be the fact.

Moreover, the FOA appears to take the position that an understanding by those skilled in the art that metal silicide should not be present when hydrogen is being used in the flow gas (as is established by the Rule 132 Declaration) is insufficient to demonstrate that Applicant was in appreciative possession of that understanding as well, this being so even though it is an indisputable fact that the illustrated ONO-type memory cell stack in Fig. 3A does not include a metal silicide layer.

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

It is respectfully submitted that the legally unsupported position of the FOA, does make reasonable sense. It is impractical to list for every method, all the things that should *not* be included.

It is well established law that the drawings constitute part of the written description. See again, Cooper Cameron Corporation v. Kvaerner Oilfield Products 291 F.3d 1317, 1323, 62 USPQ2d 1846 (Fed. Cir. 2002). It is an indisputable fact that the illustrated ONO-type memory cell stack in Fig. 3A does not include a metal silicide layer.

With regard to Claim 12, there is no showing of the recited height variation ratio in combination with the limitations of Claim 3. In re Aller does not stand for the proposition that all discoveries are obvious. On the other hand, according to In re Ochiai, 37 USPQ.2d 1127 (Fed. Cir. 1995) "[S]ection 103 requires a fact-intensive comparison of the claimed process with the prior art rather than the mechanical application of one or another per se rule. See *Pleuddemann*, 910 F.2d at 827, 15 U.S.P.Q.2D at 1741").

With regard to Claim 13, there is no showing of the recited lateral sidewall breakdown voltages.

With regard to Claim 14, there is no showing of the recited larger erase speed relative to that obtained with a sidewall dielectric formed by a dichlorosilane-based HTO process.

With regard to Claim 15, there is no showing of the recited forming of a further and supplemental sidewall dielectric by a non-ISSG oxidation process after said dry ISSG process. You does not teach or suggest forming a sidewall by dry ISSG. Wang also does not teach or suggest forming the recited first sidewall by dry ISSG.

With regard to Claim 21, there is no showing of the recited setting of the O2 flow rate over the range of about 3slm to about 10slm.

With regard to Claim 22, there is no showing of the recited additional setting of the H2 flow rate over the range of about 0.1slm to about 1slm.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

With regard to Claim 23, there is no showing of the recited short lived oxygen radicals. Xing directs the ordinary artisan to have long lived radicals. So does Wang for the purpose of achieving peak radical concentration. The ability of the FOA to appreciate the

physics of the invention in hindsight does not make for a prima facie case. See for example, In re Fine, 837 F.2d 1071; 5 USPQ.2d 1596, (Fed Cir. 1988) {"To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." W.L. Gore, 721 F.2d at 1553, 220 USPQ at 312-13. It is essential that "the decisionmaker forget what he or she has been taught at trial about the claimed invention and cast the mind back to the time the invention was made . . . to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." Id. One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to depreciate the claimed invention."}. See also In re Kahn, 78 USPQ.2d 1329, (Fed. Cir. 2006), rehearing, en banc, denied (Fed. Cir., June 1, 2006) {"the Board reiterated that the rationale of [its earlier] decision was correct and explained that motivation "clearly is based upon a prospective look at the state of the art."" [emphasis added.]}

With regard to Claim 24, there is no showing of the recited consistent, predefined performance characteristics.

With regard to Claim 26, there is no showing of the recited instability or extinguishment of the hydrogen flame.

Response After Final to Second §112 Rejection

If understood correctly, the FOA takes the position with regard to Claim 26 ("constrained to below a volumetric flow ratio of H_2 to O_2 at which formation of a hydrogen flame due to the presence of H_2 is at least unstable if not that the flame is extinguished or unignited due to insufficient presence of H_2) that the specification as filed fails to provide support for this.

However, it is undisputable that paragraph [0040] of the specification states:

> As used herein, the so-called, thermal oxidation with a wet combination of O_2 and H_2 refers to a process where a supplied stream of H_2 is burned (made to

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

> produce an invisible flame) in the presence of flowing O_2 to thereby form high temperature water vapor (H_2O) where the volumetric flow ratio of H_2/O_2 (each in terms of sccm) is in the range of 1.0 to 1.8. It is outside of conventional, mass-production practice to reduce the H_2/O_2 volumetric flow ratio below this range (more specifically, below 0.3) because the flame may become unstable at lower values of the ratio.

What appears to be in dispute though, is how a person of ordinary skill in the art would read this text and what inferences such a person would take away from it. Applicant respectfully submits that a person skilled in the art would understand that if the H_2/O_2 ratio is zero (0), that there can be no flame because there is no hydrogen present to be burned. Applicant respectfully submits that a person skilled in the art would understand that if the H_2/O_2 ratio starts off in the conventional range of 1.0 to 1.8 where the flame has been ignited (the hydrogen fire was started) and the H_2/O_2 ratio is reduced continuously until it is zero (0), there will be a value where the flame starts to become "unstable" and a lower value where the flame finally goes out. The concept of there being a value where the flame is "unstable" is clearly presented in specification paragraph [0040] as shown above. The concept that the flame will be extinguished as the H_2/O_2 ratio is reduced continuously until it is zero (0) is inherent and did not have to be spelled out for those skilled in the art. Thus a person skilled in the art will readily understand that Applicant was in appreciative possession of the idea of using a low H_2/O_2 ratio where "formation of a hydrogen flame due to the presence of [the low relative amount of] H_2 is at least unstable if not that the flame is extinguished or unignited due to insufficient presence of H_2". Extinction of the flame is inherent as the H_2/O_2 ratio is reduced below the flame instability and towards being essentially zero (0). The specification clearly mentions being "below" the conventional range.

With regard to Claim 27, there is no showing of presence in the prior art of the recited instability of the hydrogen flame being assured on a mass production basis.

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

If understood correctly, the FOA appears to take the position with regard to Claim 27 ("is constrained to below a volumetric flow ratio of H_2 to O_2 at which stable ignition of a hydrogen flame due to the presence of H_2 is assured on a mass production basis") that the specification as filed fails to provide support for this. However, it is undisputable that paragraph [0040] of the specification states (repeating from the above with emphasis added): "It is outside of conventional, mass-production practice to reduce the H_2/O_2 volumetric flow ratio below this range (more specifically, below 0.3) because the flame may become unstable at lower values of the ratio". It is respectfully submitted that this passage provides adequate support for Claim 27.

Response After Final to Examiner's Response to Arguments re "for example"

If understood correctly, the FOA appears to take the position with regard to the You '613 language: "for example a dry oxidation process" that a person of ordinary skill in the art would interpret this passage to mean, "I the ordinary artisan can use any of an infinite number of different oxidation processes as I please while the stated one-and-only example of "dry" oxidation is merely a nonbinding suggestion which I can readily choose to ignore," --to sort of paraphrase the thought process of the hypothetical artisan.

The FOA challenges Applicant's assertion with regard to the You '613 language: "for example a dry oxidation process" that a person of ordinary skill in the art would interpret this passage to mean that dry (no hydrogen) oxidation must be used. Applicant respectfully re-asserts that, yes, the person of ordinary skill in the art would interpret this passage to mean that dry (no hydrogen) oxidation must be used. This is backed up by evidence, by the submitted Rule 132 Declaration.

Interpretation of a prior art document is an issue of fact. Prior art documents must be interpreted through the eyes of a skilled artisan at the relevant time and not through the eyes of an unskilled layman. Al Site Corp v. VSI International 50 USPQ2d 1161 (fed, Cir. 1999) (In the first place, the level of skill in the art is a prism or lens through which a judge or jury views the prior art and the claimed invention. This reference point prevents these deciders from using their own insight or, worse yet, hindsight, to gauge obviousness.)

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Of course, an untrained layperson may easily say to himself: "Oxidation is oxidation, what's the difference? One is like the next." But this is where the insight of the skilled artisan overshadows the simple mindedness of the unskilled layperson. Oxidation is not just another word. There all sorts of nuances and fine points to oxidation as has been made clear in the record of the present prosecution by way of the Rule 132 declaration and by way of attorney arguments.

The FOA appears to emphasize the phrase "for example" in You '613 from a purely linguistic view point, rather from the view point of the skilled artisan. The FOA appears to see many possibilities opened up to the ordinary artisan by You's silence; by the fact that You '613 does not come out and explicitly say, "Warning, do not use anything but dry oxidation." This denies the realities of the patent drafting process. Persons skilled in the art understand that patents are generally drafted by attorneys and not directly by the engineers/scientists. You '613 clearly shows on its front cover page that a law firm was involved in its prosecution. This is a fact. No reasonable attorney/law firm will readily allow their client to write in a patent application, "Warning, do not use anything but dry oxidation." They will almost always push the inventors/engineers/scientists to include hedge language such as, "for example". If indeed there were other viable alternatives to "dry" oxidation, You et al. could have easily provided at least one more example. But You didn't. And the reason is because, technically speaking, there was none. The Rule 132 Declaration of record provides undisputed evidence that the skilled artisan would not use anything other than dry, hydrogenless oxidation due to the presence of the metal silicide (111 Fig. 2a) in You's structure. The patent examination process should be one based on science, on the realities of real world chemistry, and not on playing word games and engaging in linguistic expansionism. It is respectfully submitted that the person of ordinary skill would assign different weights to different parts of a patent document based on the knowledge that some artisans are more credible, more precise with their language and more authoritative than others. The words "for example" would be heavily discounted in this particular instance. Patent attorneys are not scientists. There are untold numbers of issued patents in the semiconductor field where clearly the attorney who wrote the text did not know the difference for example, between "thermally growing" oxide and "depositing" oxide, although in most instances the two are not at all the same. The person of skill in the art generally knows when a portion of a patent is being filled in with attorney hedge language (often unintentional misinformation due to the attorney's technical ignorance)

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

rather than with an artisan's knowledgeable provision of useful information. The "for example" in You's disclosure would be seen as mere puffery; as just smoke and mirrors put in there probably at the instance of a patent attorney who did not want the disclosure to appear to be too limiting. However, a person skilled in the art would understand that in the particular case of You '613, where metal silicide is taught as an important part of the ONO stack, the oxidation must be so limited. There is no other viable oxidation process disclosed. The only process disclosed and taught is "dry" oxidation. It is an act of hindsight to read into You '613 more than what is actually taught to the ordinary artisan.

A person skilled in the art would read You '613 as teaching away from use of anything but dry oxidation. This established in the Rule 132 of record.

Response After Final to Examiner's Response to Arguments re motivation to combine

Exactly one week after Applicant's response to final was filed (4/23/2007), the US Supreme Court handed down its KSR v. Teleflex decision (on 4/30/2007).

One thing that KSR did not do, is open the door for the PTO to ignore "away" teachings. It is still the law that when one of two references teaches away, the combination cannot be made. The Rule 132 of record establishes that You '613 would be seen by an ordinary artisan as teaching away from using anything but "dry" oxidation, in spite of insertion of the artful "for example" language in its text.

Additionally, after KSR, a new class of "common sense" decisions have been handed down by the Board of Appeals. One of them indicates that in cases where the prior art already provides a solution for a known problem (i.e. Bird's Beak) the "common sense" of the ordinary artisan would tell him to use the known solution rather than to go hunting for untested alternate solutions. **In other words, per common sense, if it ain't broke, don't fix it.**

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

See explicitly: Ex parte Rinkevich, Appeal 2007-1317, Application 09/731,623, Decided: May 29, 2007 ("Nevertheless, in KSR the Supreme Court also qualified the issue of hindsight by stating that "[r]igid preventative rules that deny fact-finders recourse to common

sense, however, are neither necessary under our case law nor consistent with it." KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 82 USPQ2d at 1397. In the instant case, we conclude that a person of ordinary skill in the art having common sense at the time of the invention would not have reasonably looked to Wu to solve *a problem already solved by Savill*." [*Emphasis added.*])

In the instant case, You '613 provides a solution, namely to nitridate the surfaces of the ONO sidewalls so that no sidewall layer remains exposed during the subsequent dry oxidation but rather so that the nitride protectively coats all the layers against rapid permeation of oxidizing agents into the center of the ONO stack. This aspect is also discussed in the Rule 132 of record and remains unrebutted. You '613 teaches away from having exposed surfaces. You provides a solution to Bird's Beak.

The outstanding Final Office Action (FOA) appears to take the position that Applicant has not rebutted the proffered motivation: "a dry ISSG provides *excellent thickness control* and the *thermal budget* can be reduced". This position, namely that Applicant has not contested the assertion, is not true. As shown above, Applicant has thoroughly rebutted each prong of the two prong allegation of a justifying motivation.

In view of the above, there is ample reason to reverse the rejection as being based on an improper motivation statement; one that has been rebutted by expert testimony. The declarant, Mr. Chen is hardly a lightweight in the field. He has a PhD degree in chemistry. He co-authored a number of professional papers in the field. He is a named co-inventor on a number of patents issued in the field. His declaration should not be summarily dismissed.

With regard to summary dismissal of Rule 132 declarations, please see again In re Alton, 37 U.S.P.Q.2d 1578, 1582-1584 (Fed. Cir. 1996):

> [The] Examiner's final rejection ... contained **two errors: (1)** viewing the [expert's] declaration [respecting the adequate disclosure issue as being merely an] opinion ... addressing a question of law rather than [providing factual testimony pertaining to] a question of fact; **and (2) the summary dismissal of the [expert's] declaration**, without an adequate explanation of why the declaration failed to rebut the [rejection] ... [With regard to item (1), we read the expert's] declaration [as] offering factual evidence in an attempt to explain *why* one of ordinary skill in the art would have understood the specification to describe [adequately the subject matter at question] .... [With regard to item (2), as the burden of coming forward with arguments and evidence shifts back

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

> and forth from first being on the Examiner to present a prima facie case and then to the Applicant to rebut; **after such rebuttal] evidence or argument is submitted by the Applicant in response, patentability [must be] determined on the totality of the record**, by a preponderance of the evidence with due consideration to persuasiveness of argument. ... [In this case, **the Examiner committed error] by failing to articulate adequate reasons to rebut the [expert's] declaration** [which failure means that the PTO has] failed to consider the totality of the record ...

[Emphasis and bracketed text added. Some language skipped over for sake of brevity.]

It is respectfully submitted that, when the totality of weights of "evidence" are placed on the opposing scales of justice in his case (as they should be) and reconsidered with regard to teachings and motivations, the preponderance of evidence clearly tips in favor of a finding nonobviousness and patentability.

CONCLUSION

In light of the foregoing, Applicant once again respectfully requests that the outstanding grounds of rejection be reversed and the claims be reconsidered in light of the evidence on record and allowed.

The Director is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional filings (e.g. of Appeal Brief) for additional claims, which may be required for maintaining pendancy of the application and/or of the appeal.

LAW OFFICES OF
MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

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Gideon Gimlan

Signature: [signature]

Respectfully submitted,

[signature]

Gideon Gimlan
Attorney for Applicants
Reg. No. 31,955

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Tel: (408) 392-9250

****

LAW OFFICES OF
MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

(viii) Claims appendix.

An appendix containing a copy of the claims involved in the appeal.

(Claims 1-15, 21-23, 24-28):

Claim 1 (*Previously Presented*): A method of forming sidewall dielectric on an ONO-type memory cell stack where at least one sidewall of the ONO-type memory cell stack includes at least three exposed material layers with at least two of the exposed material layers being respectively composed of an oxide and an oxidizable material disposed adjacent to the oxide, the method comprising:

(a) subjecting the at least one sidewall to a dry ISSG process (In-Situ Steam Generation) where the dry ISSG process comprises:

(a.1) flowing molecular oxygen (O_2) towards the stack; and

(a.2) flowing molecular hydrogen (H_2) towards the stack, where the volumetric flow ratio of the H_2 to the O_2 is less than about 0.2.

Claim 2 (*Original*): The sidewall dielectric forming method of Claim 1 wherein:

(a.2a) said volumetric flow ratio of H_2/O_2 is less than about 0.1.

Claim 3 (*Original*): The sidewall dielectric forming method of Claim 1 wherein:

(a.2a) said volumetric flow ratio of H_2/O_2 is equal to, or less than, about 0.02.

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Claim 4 (*Previously Presented*): The sidewall dielectric forming method of Claim 3 and further comprising:

(b) rapidly heating the flowing oxygen (O_2) and flowing hydrogen (H_2) to a temperature in the range of about 850°C to about 1050°C as they flow towards said at least one sidewall.

Claim 5 (*Previously Presented*): The sidewall dielectric forming method of Claim 3 and further comprising:

(b) continuing the subjecting of the at least one sidewall to the dry ISSG process for a duration selected from the range of about 20 seconds to about 300 seconds.

Claim 6 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 and further comprising:

(a.1a) varying the O_2 flow rate over the range of about 3slm to about 10slm (ten standard liters per minute).

Claim 7 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 and further comprising:

(a.2a) varying the H_2 flow rate over the range of about 0.1slm to about 1slm.

Claim 8 (*Previously Presented*): The sidewall dielectric forming method of Claim 3 and further comprising:

(b) establishing a chamber pressure for the flowing oxygen (O_2) and flowing hydrogen (H_2) in the range of about 5 Torr to about 50 Torr.

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Claim 9 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 and further wherein:

(b) said at least three exposed material layers of the ONO-type memory cell stack includes:

(b.1) a first silicon nitride layer;

(b.2) a first silicon layer; and

(b.3) a first silicon oxide layer adjacent to the first silicon layer.

Claim 10 (*Previously Presented*): The sidewall dielectric forming method of Claim 9 and further wherein said at least three exposed material layers of the ONO-type memory cell stack includes:

(b.4) a second silicon layer;

(b.5) a second silicon oxide layer;

(b.6) a tunnel dielectric layer;

(b.7) wherein the first silicon nitride layer is interposed between the first and second silicon oxide layers; and

(b.8) wherein the combination of the first and second silicon oxide layers and the first silicon nitride layer is interposed between the first and second silicon layers.

Claim 11 (*Previously Presented*): The sidewall dielectric forming method of Claim 10 and further wherein said at least three exposed material layers of the ONO-type memory cell stack includes:

(b.9) a second silicon nitride layer; disposed above the first silicon layer; and further wherein:

said ONO-type memory cell stack does not include a metal silicide layer.

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San Jose, CA 95110
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Claim 12 (*Previously Presented*): The sidewall dielectric forming method of Claim 3 and further wherein:

a height variation ratio, $R_H = H_{outer}/H_{inner}$, determined for the ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process, is about 1.20 or less, where H_{inner} represents a stack height at a lateral position in the stack that is spaced away from the stack edges and where H_{outer} represents a stack height at a lateral position near or at one of the stack edges.

Claim 13 (*Previously Presented*): The sidewall dielectric forming method of Claim 10 and further wherein lateral sidewall breakdown voltages are substantially uniform along the height of the ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process.

Claim 14 (*Previously Presented*): The sidewall dielectric forming method of Claim 10 and further wherein a larger erase speed is obtained in a memory cell having said ONO-type memory cell stack after formation of the sidewall dielectric by the dry ISSG process, where the larger erase speed is larger than a corresponding erase speed obtained in a corresponding memory cell having an ONO-type memory cell stack with sidewall dielectric formed by a dichlorosilane-based HTO process.

Claim 15 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 and further comprising:

(b) after said dry ISSG process, forming further and supplemental sidewall dielectric by a non-ISSG oxidation process.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

Claims 16-20: (*Canceled*).

Claim 21 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 and further comprising:

(a.1a) setting the O_2 flow rate over the range of about 3slm to about 10slm (ten standard liters per minute).

Claim 22 (*Previously Presented*): The sidewall dielectric forming method of Claim 21 and further comprising:

(a.2a) setting the H_2 flow rate over the range of about 0.1slm to about 1slm.

Claim 23 (*Previously Presented*): A method of forming sidewall dielectric on an ONO-type memory cell stack where at least one sidewall of the ONO-type memory cell stack includes at least three exposed material layers with at least two of the exposed material layers being respectively composed of an oxide and an oxidizable material disposed adjacent to the oxide, the method comprising:

(a) subjecting the at least three exposed material layers of the sidewall of the ONO-type memory cell stack to a dry ISSG process (In-Situ Steam Generation) where the dry ISSG process generates short lived oxygen radicals whose reactivity extinguishes before the short lived oxygen radicals are able to permeate laterally as deep into said exposed oxide material of the ONO-type memory cell stack and oxidize materials therein as would the reactive oxygen of a dichlorosilane-based High Temperature Oxidation (HTO) process applied to an essentially same ONO-type memory cell stack.

Claim 24 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 wherein method is part of mass production process that mass produces integrated circuits to have consistent, predefined performance characteristics.

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Claim 25 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 wherein said oxidizable material has a sacrificial nitride layer disposed thereon and the method further comprises:

(b) stripping off the sacrificial nitride layer after performance of said step (a) of subjecting the at least one sidewall to the dry ISSG process.

Claim 26 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 wherein said step (a.2) of flowing the molecular hydrogen (H_2) towards the stack is constrained to below a volumetric flow ratio of H_2 to O_2 at which formation of a hydrogen flame due to the presence of H_2 is at least unstable if not that the flame is extinguished or unignited due to insufficient presence of H_2.

Claim 27 (*Previously Presented*): The sidewall dielectric forming method of Claim 1 wherein said step (a.2) of flowing the molecular hydrogen (H_2) towards the stack is constrained to below a volumetric flow ratio of H_2 to O_2 at which stable ignition of a hydrogen flame due to the presence of H_2 is assured on a mass production basis.

Claim 28 (*Previously Presented*): The sidewall dielectric forming method of Claim 15 wherein said non-ISSG oxidation process includes use of dichlorosilane.

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MacPherson, Kwok, Chen & Heid LLP
2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

(ix) Evidence Appendix

An appendix containing copies of any evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner. Reference to unentered evidence is not permitted in the brief. See § 41.33 for treatment of evidence submitted after appeal. This appendix may also include copies of the evidence relied upon by the examiner as to grounds of rejection to be reviewed on appeal.

9.1: Declaration of Chiliang (Larry) Chen Traversing Grounds of Rejection Pursuant to 37 C.F.R. §1.132

This evidence (copy attached) submitted pursuant to §1.132 was filed in Nov. 2006 and accepted as part of the record by the examiner in the Office action of 1/26/2007 at page 6 paragraph 6 thereof.

9.2 A copy (attached) of You 6,706,613

9.3 A copy (attached) of Wang 2005/0110102

(x) Related proceedings (NONE) appendix. An appendix containing copies of decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of this section.

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2033 Gateway Place, Suite 400
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Zhong Dong et al		
Assignee:	ProMOS Tech. Inc.		
Title:	METHOD OF FORMING ONO-TYPE SIDEWALL WITH REDUCED BIRD'S BEAK		
Serial No.:	10/821,100	Filing Date:	April 7, 2004
Examiner:	Vu David	Group Art Unit:	2818
Docket No.:	M-15295 US	Confirmation No.:	8965

Santa Clara, California

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Declaration of Chiliang (Larry) Chen Traversing Grounds of Rejection Pursuant to 37 C.F.R. §1.132

Dear Sir:

I, Chiliang ("Larry") Chen, declare as follows:

1. My current residence is in Sunnyvale, California.

2. OCCUPATIONAL AND EDUCATIONAL CREDENTIALS

2a. I am currently an employee of Mosel Vitelic Corp. (MVC, Santa Clara, CA facility). MVC is an affiliate of the assignee of the above-identified patent application (ProMos Tech. Inc.). My current position at MVC is Engineering Manager (from 2004 to the present). I previously held the position of Staff Engineer at MVC (2002-2004). In both positions, I was responsible for development of flash memory chips in the 70nm, 0.12μm, and 0.18μm channel length regimes. This work included overseeing development of HDP-CVD recipes for STI gap-fill to meet isolation requirements; overseeing development of sidewall

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

oxidation methods (including ISSG) for use in reduction of Bird's Beak; overseeing development of recipes for nitridizing oxide layers in ONO stacks; and overseeing development of RTP annealing recipes and selection of dielectric capacitor materials for use in mass production fabricating of ONO stacks. A number of the named inventors work with me at MVC in the Northern California research facility.

2b. I personally have approximately 11 years of work related experience in the field of forming dielectric insulating layers in mass-produced integrated circuits, and particularly in the problems of fabricating dielectric layers and reducing or avoiding Bird's Beak. Prior to joining MVC, I worked at Applied Materials (Santa Clara, CA) and held the positions there of Member of Technical Staff (1999-2002), Applications Lab Manger (1997-1999) and Senior Process Engineer (1995-1997). Part of my work at Applied Materials involved development of advanced gate and capacitor dielectric layers by use of ALD-deposited Al2O3, LPCVD-deposited SiN and SiON, use of RTO and ISSG. In most of my work-related experiences I have been intimately involved in process related details including formation of silicon oxides and silicon nitrides by various methods including formation of ONO stacks within the context of mass production of IC's.

2c. In 1996 I was awarded a Ph. D. in Chemical Engineering from the University of Minnesota. In 1986 I received a B. S. degree in Chemical Engineering from the National Taiwan University.

2d. I co-authored a number of professional papers including: (a) *Enabling Single-Wafer Process Technologies for Reliable Ultra-thin Gate Dielectrics*, with G. Miner, G. Xing, S. J. Hyun, E. Sanchez, Y. Yokota, D. Lopes, A. Balakrishna; Electrochem. Soc. Symp. Proc. 99-10, 3 (1999); and (b) *Attainment of Low Resistivity Polycide Films Using Rapid*

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2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Thermal Annealing, with H. A. Yoon, A. Singhal, D. Lopes, G. Miner, S. Hong, Y. Maeda, M. Yamazaki, Electorchem. Soc. Symp. Proc. 99-10, 249 (1999).

2e. I am a named co-inventor on the following US patent: 6,066,836 issued May 23, 2000 and entitled: *High temperature resistive heater for a process chamber*. I am a named co-inventor on the following US patent applications: 2002/0168840 published November 14, 2002 and entitled: *Deposition of tungsten silicide films*; and 2003/0000647 published January 2, 2003 and entitled: *Substrate processing chamber*.

2f. My professional work experience and educational background make me well qualified to opine on the understandings of persons of ordinary skill in the relevant art and at the relevant times as detailed below.

3. DOCUMENTS REVIEWED

3a. In preparing for making this Declaration, I reviewed the following documents:

3.1) Originally filed patent application Ser. No. 10/821,100, filed 4/7/2004 by Zhong ("Mark") Dong et. al (hereafter also "the subject patent application");

3.2) Final Office Action (OA) of June 6, 2006 for said Ser. No. 10/821,100 and the subsequent Advisory Action of August 21, 2006;

3.3) Applicant's Response After Final August 2, 2006 of for Ser. No. 10/821,100;

3.4) You U.S. Pat. 6,706,613;

3.5) Wang U.S. Pub. 2005/0110102 (published 5/26/05 on basis of application filed 11/25/03); and

3.6) Xing U.S. Pub. 2003/0124873 (published 7/3/03).

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

4. REVIEW OF FINAL OFFICE ACTION

4a. As I am given to understand, in the Final Office Action (OA) of June 6, 2006, as well as in the Advisory Action of August 21, 2006, the examining official (hereafter "Examiner") at the U.S. Patent and Trademark Office (hereafter "PTO") asserted either expressly or by implication that a person of ordinary skill in the art at a time prior to April 7, 2004 (hereafter "critical date") would have been motivated and enabled by the teachings of You '613 in combination with other prior art teachings that demonstrate use of ISSG (e.g., Wang '102) to use a particularly dry form of ISSG (In Situ Steam Generation) for forming sidewall oxide on an ONO stack (Oxide/Nitride/Oxide dielectric stack) such as stack structure 120 of You Fig. 2B. In doing so, the ordinary artisan would reduce Bird's Beak formation, namely the oxide encroachment shown in Region "A" of You Fig. 1 between the polysilicon control gate 18 and the polysilicon floating gate 14. The Examiner appears to assert that a person of ordinary skill in the art at a time prior to the critical date would have been motivated to reduce Bird's Beak in this way because You '613 teaches to reduce Bird's Beak; and further that such an ordinary artisan would have been motivated to use a relatively dry formulation of ISSG (such as within the low end of the ranges stated in Wang '102) in place of the "dry oxidation" taught by You '613 at col. 6, lines 38-40. The motivation for using the relatively dry formulation of ISSG instead of You's fully dry thermal oxidation is stated in the Final Office Action as, **because "a dry ISSG process provides excellent thickness control and the thermal budget can be reduced"** (OA page 3, last 5 lines of first full paragraph, emphasis added). This was the general basis, as I understand it, for rejecting the then pending claims as being "obvious".

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

4b. It is to be understood that I am not opining here about the legal "patentability" of any claims, as amended or otherwise formed, and which the Applicant may be presenting

concurrently or in the future to the PTO. I am not opining about whether the legal scope of any claim includes limitations of its "preamble" (introductory paragraph) or not. My role here is that of reviewing the documents from a technical perspective and reviewing the fact-finding conclusions reached by the PTO and not the ultimate legal conclusions. As such, I will not be opining on what would have been legally "obvious" to one of ordinary skill in the art prior to the critical date. Instead I am opining, based on my education, background, and review of the above-stated materials, regarding what an ordinary artisan (at or before the critical date) would have understood from the applied prior art documents, from general knowledge in the art, and what an ordinary artisan would have been motivated to do or not do in light of such documents but without having hindsight knowledge of the invention set forth in the subject patent application.

4c. Let me begin by providing some important, detailed information about metal silicides and ISSG. It is to be noted that You '613 has a metal silicide layer (111 in Fig. 2A and 112 in Fig. 2B) as part of his ONO stack in a step prior to when sidewall oxidation begins. Then, at column 6, lines 38-40, You cautions that the oxidation should be a "dry" one. This term, "dry" indicates to the skilled artisan that there should be essentially no hydrogen in the oxidation atmosphere.

4d. There is a very good reason for why You '613 insists on a "dry" oxidation. It is not a user-bypassable option. Hydrogen tends to act as a catalyst for encouraging decomposition of metal silicides. At oxidation temperatures, the decomposition reaction: Si-M → Si + Metal will be accelerated by the presence of hydrogen. Then the oxygen in the atmosphere will oxidize the silicon and metal byproducts of the decomposition to produce electrically insulative oxides. As a result, the metal silicide layer (112 in You Fig. 2B) will be quickly covered by insulation and it will cease to function in its desired role as a metal gate contact (to

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

poly 109). Thus this constitutes one reason for why an ordinary artisan would heed the directions of You '613 and would avoid using a thermal oxidation process that includes hydrogen. In other words, because an ISSG atmosphere includes hydrogen, the ordinary artisan would see You '613 as teaching away from use of ISSG.

4e. With that first point out of the way, I wish to return to the Patent Office's reasoning as quoted and highlighted in above paragraph 4a (namely, that the motivation to use dry ISSG is because "a dry ISSG process provides excellent thickness control and the thermal budget can be reduced" (OA page 3, referring to Wang Abstract, emphasis added). In my professional opinion this statement is technically incorrect and without basis in Wang '102. Wang never promises or suggests that a "dry" version of his ISSG process will provide excellent thickness control for every situation. Moreover, a "dry" ISSG that does not have enough hydrogen flow to sustain a stable hydrogen flame will tend to increase consumption of the thermal budget rather than decreasing it. (This is so because the hydrogen flame provides localized exothermic heat, and without the flame, a non-local source of heat will probably have to be used (i.e., Rapid Thermal Heating lamps) and this will tend to hurt rather than help the thermal budget of the overall chip. More on this detail later.) With regard to universal applicability of ISSG to all situations, Wang's Abstract limits itself to saying: "Exposing the patterned silicon nitride to the oxygen radical during the RTO according to the invention significantly reduces the processing time, and reduces the thermal budget." Wang does not teach or suggest a universal applicability of his method. I could not find any instance where Wang mentions the word "excellent" or associates the "dry" end of his ranges with good thickness control or thermal budget reduction. The only instance of "control" that I found in Wang is at paragraph [0048] where he says: "Formation of thin oxide films on nitride using conventional methods follows a linear growth law. In contrast, formation of oxide [on nitride]

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2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

by ISSG is apparently diffusion controlled, as the square of oxide thickness values[,] is linearly proportional to oxidation time, and it conforms to the parabolic growth law." [Bracketed language and emphasis added]. From this, an ordinary artisan would see Wang '102 as being focused on how to form oxide (SiO) on silicon nitride (SiN). He would not see Wang '102 as suggesting that ISSG can be (or should be) used in every situation where excellent thickness control is to be maintained. As I already explained above, ISSG cannot be arbitrarily used in every arbitrary situation. If a metal silicide is present for example, the ordinary artisan should be highly motivated to not use an oxidation process that exposes the silicide to hydrogen. The ONO stack structure of You '613 constitutes such a situation. Thus, the ordinary artisan would have no motivation for combining You '613 and Wang '102.

4f. Now that I have provided some detailed technical observations regarding metal silicides and dry versus hydrogen-laden oxidation, this may be a good place in the discussion for stepping back to review some basics regarding the formation of Bird's Beak. I think this review will help to better position the teachings of You '613 relative to the context of Bird's Beak and also to show why the subject patent application discloses a method which is substantially different from that of You '613 and which is not suggested by Wang '102 either.

4g. It is well known in the art of semiconductor fabrication that oxygen molecules (O_2) can readily diffuse through conventional silicon dioxide (typically, amorphous SiO_2). In other words, silicon dioxide appears as being a relatively porous material to conventional, thermal oxidation processes. This is generally a desirable trait because it allows a thermal oxidation front to reach through to new silicon after oxide has already grown over previously exposed silicon. It is the easy permeation of high temperature oxygen through porous silicon oxide which makes the general process of thermal oxidation not only possible, but relatively fast and cost efficient in terms of energy expended for achieving the desired end result.

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

4h. The oxide-permeating (penetrating) property of oxygen during thermal oxidation becomes a problem however in situations such as that of Fig. 2A of You '613 where one or more silicon oxide layers (105 and 107) lie immediately adjacent to a silicon layer (i.e., the floating gate (FG) polysilicon 103 and the control gate (CG) poly 109 of You '613) and the oxide layer is "exposed" to the oxidation atmosphere. In such a case, the porosity of oxide layers 105, 107 allows energized oxygen to permeate laterally into the stack. As the permeating oxygen reaches the outer corners of the upper major surface of FG layer 105 and also the outer corners of the lower major surface of CG layer 109, it reacts with silicon in the corners and converts them into enlarged volumes of silicon dioxide. Volume enlargement is one of the well known attributes of thermal oxidation. This can lead to undesired mechanical strain as well as undesired alteration of geometries for the dielectric and the conductive layers around it. The undesirable outcome of corner erosion and increased strain is indicated to have occurred in region "A" of You Fig. 2. It is seen that the upper corners of FG layer 14 have been consumed and converted to oxide due to lateral oxygen permeation through ONO structure 16. The lower corners of CG layer 18 have also been consumed and converted to oxide by virtue of such lateral permeation of oxygen through the porous oxide layers of the ONO structure 16. While not shown; it is understood that the dielectric material between poly gates 14 and 18 has been strained by the undesired lateral growth of oxide. This undesirable intrusion of an enlarged-volume of oxide into a critical region of capacitive coupling is often referred to by practitioners as "Bird's Beak". It is undesirable because it alters the electrical behavior of the dielectric and of the conductors (usually polysilicon) that sandwich the interposed dielectric. The Bird's Beak problem is a notoriously old one. There has been a long felt need in the industry to come up with economic and consistent ways of preventing or reducing Bird's Beak. Numerous techniques have been tried with varying degrees of success.

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Each approach has its positive aspects and its drawbacks, particularly when practiced on a mass production line. Consistency of outcome is important during mass production.

4i. The degree to which Bird's Beak forms is dependent on numerous process specifics including but not limited to: (1) What is the crystalline structure of the oxide layer (i.e., highly amorphous or not?) through which the oxidizing agent will be permeating laterally? (2) What is the rate of permeation of the oxidizing agent? (3) What is the composition of the adjacent silicon (i.e., polycrystalline, monocrystalline, amorphous)? (4) What is the rate of oxidation of the adjacent silicon by the given oxidizing agent at the given process temperatures, pressures and reactant flow rates? Given all these variables, it is difficult for an ordinary artisan to anticipate ahead of time, and without significant experimental experience how Bird's Beak will develop under an unfamiliar type of oxidation. Silane-based (or dichlorosilane-based) HTO oxidation has been the oxidation method of choice in the industry for ONO sidewalls. The reasons why are detailed later below. As such, a significant body of experimental data already exists for how Bird's Beak forms under the specific conditions of various silane-based HTO recipes. Also, a significant body of experimental data already exists for how Bird's Beak forms under the specific conditions of older, dry oxidation methods. To the best of my knowledge and belief, very little industry-wide data was available prior to the critical date for how Bird's Beak might form under the specific conditions of various ISSG recipes. A person of ordinary skill in the art would not see ISSG as an obvious-to-try method for oxidizing ONO sidewall because the outcome is unknown without resort to undue experimentation. By contrast, the outcome for the industry-conventional silane-based HTO recipes or dry oxidation recipes is much better understood. So the person of ordinary skill would have been motivated (prior to learning of the excellent results obtained by the subject patent application) to shy away from ISSG or other forms of

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

nonstandard sidewall oxidation and to stick with the tried and true conventional methods, namely, silane-based HTO recipes. This is another reason why a person of ordinary skill would not view the teachings of You '613 as an invitation try all forms of alternate oxidations aside from the dry oxidation which You '613 has apparently already validated as providing good Bird's Beak results. It is not at all clear how ISSG or other forms of oxidation might fair (in terms of forming Bird's Beak or not and providing sufficient rate of sidewall oxidation) under the conditions of the ONO structure of You '613 where a nitride barrier covers the exterior of the ONO stack and impedes the advancement of the oxidizing agent.

4j. This is a good point to discuss the nitride coating which You '613 forms in his "pre-anneal" step of col. 6, lines 8-37. Just as it is known in the art that oxygen can diffuse easily through silicon dioxide, it is also well known that oxygen has a difficult time of diffusing through silicon nitride when conventional thermal oxidation techniques are used. Silicon nitride (stoichiometric Si_3N_4 or other compounds of silicon where many S-N bonds are formed) is often used as an "oxidation stop" or an "oxidation barrier" because of this phenomenon. It is used to stop or substantially slow the progress of an advancing oxidation front during a thermal oxidation process.

4k. In fact, prior to the critical date, it would have been very clear to an artisan of ordinary skill that You '613 teaches at col. 6, lines 8-37 to use silicon nitride as a thin diffusion barrier on the sidewall of an ONO stack for precisely this purpose; for slowing down lateral permeation of oxygen into the interior of the stack during thermal oxidation of the sidewalls of his FG/ONO/CG stack 120 of Fig. 2B. You '613 implicitly teaches at col. 6, lines 36-37 that, were it not for the S-N bonds formed in his nitrogen pre-anneal step of col. 6, lines 8-25, that "oxidizing agents" would have "penetrate[d] into the central portion of the ONO layer 108 [in other words, deep into region "A" of You Fig. 1, reaching as far as the outer

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

boundary of region "B"]" [*Bracketed text added*]. You '613 unequivocally teaches at col. 6, lines 29-35 that a film containing strong silicon-nitrogen bonds (S-N bonds) should be formed on the sidewall 102a of stack 120 before the stack is subjected to the thermal oxidation (to the "dry oxidation" of col. 6, lines 38-40). The pre-oxidation anneal in the nitrogen containing atmosphere causes the sidewalls in You's stacked gate structure 120 to be covered and protected by a thin nitride film such that they are not directly exposed to the thermal oxidation environment. In other words, You's stacked gate structure 120 does not have openly exposed oxide to serve as a gateway through which oxygen can readily enter laterally into the interior of the ONO structure to thereby quickly begin the process of Bird's Beak intrusion. You's ONO structure is covered on its sidewall with nitride before thermal "dry oxidation" is initiated at col. 6, lines 38-40. This aspect of You '613 is not ambiguous or open to reasonable debate. Instead, it is the whole basis of the invention described by You '613. You uses the thin nitride coating to slow down entry of laterally permeating oxygen into the regions between his FG and CG layers, and to thereby reduce the Bird's Beak incursion as is shown in region "C" of You Fig. 2C. Note that the amount of lateral incursion by material 116 of You Fig. 2C into the interior of the stack is substantially less than lateral incursion by material 26 of You Fig. 1.

41. Given the above, it is my opinion based on my experience and educational background that a person of ordinary skill in the art, at or before the critical date, would have understood You '613 to be clearly teaching the following:

- Do not leave an open or exposed silicon oxide surface on the sidewall of the ONO stack structure as you are about to begin thermal oxidation, but instead cover all such entrances or gateways for lateral permeation of oxygen with an oxygen diffusion barrier such as silicon nitride; and

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

- Use a dry oxidation with O2 (no hydrogen in the oxidizing atmosphere) for simultaneously oxidizing the nitride-covered sidewalls and for annealing lateral ends of the ONO structure so as to thereby relieve any mechanical stress induced by the limited amount of Bird's Beak incursion (region "C" of You Fig. 2C) that does occur.

4m. It is further my opinion based on the above that a person of ordinary skill in the art, at or before the critical date, and upon reading You '613, would have been guided away from:

- Leaving an open or exposed silicon oxide surface on the sidewall of the ONO stack structure when beginning thermal oxidation so as to thereby provide an entryway for lateral permeation of conventional oxidizing agents into the ONO structure; and

- Using a non-dry oxidation process (i.e., ISSG, wet oxidation) for oxidizing the nitride-covered sidewalls and for simultaneously annealing lateral ends of the ONO structure.

As explained above, hydrogen tends to accelerate silicide decomposition. Since You's ONO stack includes a metal silicide layer prior to commencement of the thermal oxidation, a person skilled in the art would be strongly motivated to pay heed to You's requirement for a "dry" oxidation and such an ordinary artisan would not think of instead using an oxidation process that exposes the metal silicide to hydrogen. Moreover, since it is not clear how Bird's Beak formation would proceed if a method other than dry oxidation were tried in the situation presented by You '613, an ordinary artisan would be motivated away from randomly trying alternate methods of sidewall oxidation. Accordingly, You '613 guides the ordinary artisan

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

away from contemplating the use of ISSG or other non-dry, thermal oxidation processes. Even if for sake of argument, You '613 might be seen as suggesting a try of wet oxidation (see col. 2, line 16 where You '613 mentions wet oxidation (H_2O) as part of the general method for oxidizing exposed silicon), that alone does not recommend ISSG, and more specifically dry ISSG as an alternate method to be tried. In other words, You '613 nowhere recommends that dry ISSG be specifically tried as a method for reducing Bird's Beak and Wang '102 nowhere recommends that dry ISSG be specifically tried as a method for reducing Bird's Beak.

Thermal Oxidation Processes are Not All the Same and Equivalently Interchangeable

5a. The specification of the subject patent application indicates that the ONO sidewall is conventionally oxidized with a silane-based HTO process (High Temperature Oxidation) and that Birds' Beak results. See for example paragraph [0039]: "Another problem with the conventional oxidation processes (e.g., HTO) is that the heated molecular oxidizing agents (e.g., O2) readily diffuse through the SiO layers ... to thereby attack the underside of Poly ... A set of Bird's Beak formations ... develop as a result of incursion of the molecular oxidizing agents (e.g., O2) through the SiO layers 114, 116." [*Some detailed text clipped out here.*]

5b. What the specification perhaps leaves out is a detailed explanation of what motivates the ordinary artisan to conventionally rely on a relatively water-free, High Temperature Oxidation (HTO) process such as the exothermic DCS+N2O reaction described in the specification as opposed to other possible methods of forming sidewall oxide. Not all forms of creating oxide are the same. A person of ordinary skill in the art would not arbitrarily substitute one for the other or pick arbitrary operating parameters for any specific approach.

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

As I already explained, a hydrogen-free atmosphere should be used when a metal silicide contact layer has already been formed as part of the stack. Careful attention to Fig. 3A of the subject patent application will show that the Poly-2 layer (318) is not yet covered by a metal contact layer, but instead has a silicon nitride pad layer (319) above it as the ISSG sidewall-oxidizing process (320) is initiated. The specification does not highlight these subtleties. However, at paragraph [0061] it indicates that "the pad silicon nitride 319' will generally still be present at the time of the supplemental HTO oxidation 380 and that it will be stripped off by HF etch or otherwise after that."

5c. While it does not provide every minutiae of detail, to its credit, the specification of the subject patent application does explain at specification paragraph [0040] one further aspect that would de-motivate an ordinary artisan from using a dry ISSG, to wit:

> [0040] Conventional oxidation for producing sidewall dielectric is not limited to HTO (High Temperature Oxidation). Other conventional methods that have been used include thermal oxidation with **dry O_2** (molecular oxygen) and thermal oxidation with a **wet combination** of O_2 and H_2 (molecular hydrogen) and thermal oxidation **with water vapor** (H_2O). As used herein, the so-called, thermal oxidation with a wet combination of O_2 and H_2 refers to a process where a supplied stream of H_2 is burned (made to produce an invisible flame) in the presence of flowing O_2 to thereby form **high temperature** water vapor (H_2O) where the volumetric flow ratio of H_2/O_2 (each in terms of sccm) is in the range of *1.0 to 1.8*. It is outside of conventional, **mass-production** practice to reduce the H_2/O_2 volumetric flow ratio below this range (more specifically, *below 0.3*) **because the flame may become unstable** at lower values of the ratio. [*Emphasis added.*]

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2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

5c. The reasons why the ordinary artisan would usually want to assure a consistent ignition of the hydrogen flame immediately adjacent to the surface undergoing oxidation are many fold. Xing '873 was used by the Examiner as a source of alleged evidence regarding

radical lifetime (and I will address that issue later). Here I point to Xing paragraph [0039] as showing that the ordinary artisan will conventionally wish to "ignite" the gas containing the oxygen and hydrogen and that the ordinary artisan will conventionally want the surface that is undergoing oxidation is to serve as the "ignition source". This localized ignition of the hydrogen and oxygen sources provides selective application of exothermically-generated heat to just the right places and assures that a large number of oxygen radicals will be present at those places. Thus it is against conventional thinking to try an ISSG recipe where the volumetric flow ratio of H_2/O_2 (each in terms of sccm) is in a range below 1.0 (below unity). The reasons why are detailed immediately below.

5d. Semiconductor fabrication can consume large amounts of energy and process steps can take significant time. It is highly desirable to not waste energy by uselessly heating parts of the wafer that do not need to be heated, especially if this is going to eat into their thermal budgets. It is highly desirable to not waste time by using a process that is relatively slow and fails to provide an adequate supply of oxygen radicals to the place where they are desired. It is also highly desirable to assure consistent results during mass production. In view of this, the person of ordinary skill would want to avoid a non-exothermic ISSG process where there may not be sufficient H_2 flow to assure a consistent and stable hydrogen flame and to thus assure consistent production of exothermic heat generation at the sidewall surface. Note that Xing '873 recommends approximately 10% H_2 at paragraph [0033]. Note that working Example 3 of Wang '102 is a relatively wet formulation where at paragraph [0047] of Wang the disclosed ISSG process has an H_2/H_2+O_2 ratio of about 33% and it is being used to produce a reduced thickness disparity: roughly 0.75 to 1.0 (SiN/Si oxidations) where such a reduced disparity is Wang's goal. Wang '102 cautions that "the ISSG process depends upon

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

using process pressure, flow rate and **temperature** in the chamber within specified ranges. ... [I]n some embodiments the following parameters can be effective: temperature in the range about 800°C to about 1000°C; pressure in the range about 1 torr to about 20 torr; flow rate of H_2+O_2 in the range about 1 slm to about 40 slm. The ratio of H_2/H_2+O_2 is in the range about 0.1% to about 40%. " (at [0032] *Emphasis and bracketed text added.*] Xing '873 also explains at paragraph [0025] that pressure is important and Xing '873 recommends low pressure for the purpose of lengthening the lifetime of the oxygen radicals so that more of them will participate in Xing's anneal process.

5e. Given the cumulative effect of these teachings in the prior art, it would be understood by a person skilled in the art that the low end of the H_2/H_2+O_2 range in Wang '102 (namely about 0.1%) would not be expected to produce an exothermic flame at conventional pressures and thus is not recommended; whereas the more "usual" and preferable range of "5% to 33%" recited at Wang paragraph [0018] would be more likely to do so. And the ordinary artisan would conventionally want to ignite a hydrogen flame at the surface undergoing oxidation for at least the reasons given above.

5f. Wang '102 does not suggest his process as a means for reducing Bird's Beak, but rather as a means for reducing oxidation thickness disparity when oxide and nitride are being simultaneously oxidized. Thickness disparity is not at all the same thing as Bird's Beak . Thus, after having read Wang '102, a person of ordinary skill would not see any relation between what Wang '102 teaches and the problem of reducing Bird's Beak.

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2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

5g. Bird's Beak does not occur from the fact that SiN and Si are being simultaneously oxidized. It occurs because oxygen permeates laterally and rapidly through a relatively porous

layer of oxide that is situated immediately adjacent to a silicon layer and the oxygen is thus able to attack the adjacent silicon layer and oxidize it.

5h. It is noted Wang has an exposed edge of his TOX layer 424 in Fig. 4E but no overlying polysilicon. Layer 426/427 is nitride. Bulging oxide growth 434 indicates volume enlargement as silicon implant region 432 and substrate are thermally oxidized. Wang provides no suggestion that a relatively dry ISSG might reduce lateral advancement of an oxidation front due to reduced lifespan of oxygen radicals and that this may in turn provide a useful solution to the long known and not fully solved, Bird's Beak problem. It seems to me that the Patent Office is copying the idea of using dry ISSG for Birds' Beak out of the subject patent application and then projecting it by way of hindsight into Wang '102 at the portion of OA page 3 where they mention Xing '873 as evidence of the state of the art.

5i. However, my review of Xing '873 shows no place where Xing suggests that the relatively short lifetime of oxygen radicals may be usefully applied to the problem of Bird's Beak. Quite the opposite. At paragraph [0025] Xing '873 teaches that the relatively short lifetime of oxygen radicals is a problem to be overcome by using low pressure so that more, not less, oxygen radicals will penetrate into the region undergoing his anneal process. The goal in Xing '873 is, of course, to increase the number of oxygen bonds per steps 204 and 210 of his Fig. 2. The ISSG process is used in Xing '873 only to enhance oxidation through the top major surfaces of oxide layers 408 and 412 of his ONO structure 414 (see Fig. 4E). This is evidenced by paragraph [0037] of Xing '873 wherein the stack is not lithographically patterned and etched until after all the ISSG operations have been performed. Thus Xing '873 teaches to perform ISSG only before the ONO stack is lithographically patterned and etched. This guides away from the teachings of You '613 wherein "dry" oxidation is performed after a metal silicide layer has been formed and after the stack has been etched. (As a subtle aside,

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

note that the tunnel oxide 404 of Xing Fig. 4B is not exposed to hydrogen incursion from the ISSG anneal (step 204) because the edge of TOX layer 404 is first sealed by an HTO oxidation step (202) that forms the bulk of first oxide layer 408.)

5j. Paragraph [0037] of Xing '873 teaches that "standard processing technique[s]" are to be used to complete fabrication. The ordinary artisan would interpret this to include the conventional, silane-base HTO oxidation of the stack sidewalls. The subject patent application explains at specification paragraph [0041] why the conventional sidewall oxidation process is an HTO one that uses DCS (or silane), as follows:

> [0041] ... the conventional, sidewall oxidizing process is HTO (High Temperature Oxidation) as is schematically indicated at 120. One particular HTO process flows **DCS (dichlorosilane) and nitrous oxide (N_2O)** over the exposed ONO memory cell stacks 110 (only one shown) in order to trigger an exothermic reaction which releases molecular oxidizing agents (e.g., O_2) along the exposed sidewalls of the ONO towers 110. The DCS plus N_2O reaction simultaneously decomposes the DCS to provide silicon atoms for deposition and oxidation along the tower sidewalls. An encasing silicon oxide layer (not shown, see instead 250 of Fig. 2A) is quickly formed. Such quick formation is conventionally desired because the rapidity of the sidewall dielectric formation helps to **reduce fabrication costs for mass produced devices. It also helps in minimizing thermal budget problems**. ... [*Emphasis added.*]

5k. The ordinary artisan would agree that the emphasis is on having a reliable and consistent method for use in mass production for assuredly maintaining an exothermic reaction that releases heat in situ at the desired location (at the sidewall of the ONO structure). This is why DCS and N2O are used as the method of choice in the industry; because they deliver almost all of the desirable attributes; except of course, that of preventing Bird's Beak (see the rest of paragraph [0041] in the specification).

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

51. The ordinary artisan would also know and agree with the proposition in the specification that an H_2/O_2 volumetric flow ratio of below a normal range (more specifically, below 0.3) is not to be used for generating exothermic heat in ISSG because the hydrogen flame may become unstable or nonexistent at lower values of the ratio and then the desired exothermic reaction may fail to consistently take place if at all. Some patent applications such as Wang 2005/0110102 may recite wide ranges of values for the H_2/O_2 mixture. However, the ordinary artisan would know to discount the extremes of these ranges as being mere puffery and not truly a workable or "usual" range to operate in. There would be no advantage to operating in the questionable extremes (in so far as one not knowing of the present invention is concerned) and there would be all the risk of losing the exothermic flame and then losing the advantage of in-situ heat generation and of process consistency. Any isolated document can recite wide and unrealistic ranges. That does not mean that a person of ordinary skill will blindly accept the ranges of a single document as being credible. Instead, the ordinary artisan would, like any reasonable person with appropriate training, seek to discover what the mainstream of teachings in the art relate to him and would follow that mainstream of conventional guidance. In the present situation, the subject patent application correctly indicates that the mainstream thinking prior to the critical date was to keep the volumetric flow ratio of H_2/O_2 (each in terms of sccm) in an ISSG process in a range above 1.0 (above unity) or at least above 0.3 given that the flame is known to become unstable or extinguished below such levels (i.e., below 0.3). (Note that an H_2/O_2 ratio of 0.3 becomes an $H_2/(O_2 + H_2)$ ratio of about 0.23; or more generally that an H_2/O_2 ratio of x becomes an $H_2/(O_2 + H_2)$ ratio of $x/(1+x)$ so that, as x approaches unity, the value of $x/(1+x)$ approaches 50%.)

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

5m. With regard to supplementing a dry ISSG step with a DCS HTO step, certainly the ordinary artisan would not have known of the idea related at paragraphs [0055]-[0056] of the subject patent application, namely, to supplement the dry ISSG with a DCS HTO. The reason for going through the complication of performing a dry ISSG and then a conventional HTO is to gain benefit of the unexpected result that short-lived oxygen does not permeate deep into the stack during the dry ISSG. At OA page 3 (where the reference to Xing '873 is made), the Final Office Action appears to imply that the ordinary artisan would have seen the connection between the normally short lifetimes of oxygen radicals (as may occur for example during ISSG) and the problem of Bird's Beak. I have carefully reviewed You '613, Wang '102 and Xing '873 looking for a place where any of these references might provide a hint of such a connection and I have found none. In my professional opinion, a person of ordinary skill in the art could not have seen such a connection. The connection (as disclosed only in the subject patent application) and the desirable results of reduced Bird's Beak are a surprise.

5n. At this point I am probably straying dangerously close to opining on the legal concept of "nonobviousness". So I stop here and summarize my conclusions as follows.

MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

6. Summary

6a. It is my opinion that the Final Office action of June 6, 2006 for the subject patent application contains numerous errors of fact finding as detailed above and it does not present to me a convincing prima facie, factual case of unpatentability based on the prior art that is cited. You '613 does not teach or suggest to the ordinary artisan that the "dry" oxidation of his nitride-coated ONO stack should be replaced by a hydrogen-containing oxidation of an uncoated (exposed) ONO stack. The covering of You '613's ONO stack with a nitride coating prior to performance of the "dry" oxidation is a vital part of what You '613 teaches. A person of ordinary skill would not have been guided or motivated by You '613 to do something different, especially to leave the stack "exposed" and to use a hydrogen-containing atmosphere for generating sidewall oxide.

6b. Wang '102 does not teach or suggest to the ordinary artisan that ISSG should be used in place of another oxidation process (i.e., dry oxidation) in any and every situation. Wang '102 is limited to the situation where it is just oxide and nitride that are to be simultaneously exposed to an oxidizing environment and it is desirable to reduce oxidation thickness disparity. Wang '102 cannot be logically combined with You '613 because You has a metal silicide layer.

6c. Xing '873 guides the ordinary artisan toward assuring that a large number of long-lived oxygen radicals should be generated at the surface that is undergoing ISSG oxidation and that sufficient hydrogen be present to assure ignition of the hydrogen flame.

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2033 Gateway Place
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San Jose, CA 95110
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6d. Prior to the critical date, a person of ordinary skill in the art could not have reasonably seen a logical connection between the disparate teachings of You '613, Wang '102 and Xing '873 that would motivate the artisan to combine two or more of these teachings

together. None of these prior art documents provide a suggestion that short-lived oxygen radicals might result in reduced Bird's Beak formation. Of course, with hindsight and after-the-fact knowledge of the successful experiments performed by the present inventors (see experimental results of Figs. 4A-4C of the subject patent application) one can then see the connection and surmise as to the probable cause and effect. However, before that, the connection between Bird's Beak and short-lived radicals was not seen. It was a surprise revelation.

6e. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 1st day of November in the year 2006

at Santa Clara, California.

(Signature)

Chiliang (Larry) Chen

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MacPherson Kwok Chen & Heid LLP
2033 Gateway Place
Suite 400
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

US006706613B2

(12) **United States Patent**
You et al.

(10) **Patent No.: US 6,706,613 B2**
(45) **Date of Patent: Mar. 16, 2004**

(54) **METHODS FOR MANUFACTURING STACKED GATES INCLUDING OXIDE/NITRIDE/OXIDE (ONO) INTERLAYER DIELECTRICS USING PRE-ANNEALING AND/OR POST-ANNEALING IN NITROGEN**

(75) Inventors: **Young-Sub You**, Gyeonggi-do (KR); **Hun-Hyeoung Lim**, Gyeonggi-do (KR); **Sang-Hoon Lee**, Seoul (KR); **Woo-Sung Lee**, Gyeonggi-do (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/359,789**

(22) Filed: **Feb. 6, 2003**

(65) **Prior Publication Data**

US 2004/0029354 A1 Feb. 12, 2004

(30) **Foreign Application Priority Data**

Aug. 7, 2002 (KR) 2002-0046612

(51) **Int. Cl.**[7] **H01L 21/76**

(52) **U.S. Cl.** **438/424**; 438/694

(58) **Field of Search** 438/296, 424, 438/435, 700, 694, 742, 721–722

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Primary Examiner—David Nelms
Assistant Examiner—David Vu
(74) *Attorney, Agent, or Firm*—Myers Bigel Sibley & Sajovec

(57) **ABSTRACT**

A semiconductor device including a stacked gate having stacked gate sidewalls and an oxide/nitride/oxide (ONO) interlayer dielectric is manufactured by pre-annealing the stacked gate in a first atmosphere that includes nitrogen. At least a portion of the stacked gate sidewalls of the stacked gate that has been pre-annealed is oxidized. Post-annealing is then performed on the stacked gate including the stacked gate sidewalls that have been oxidized, in a second atmosphere that includes nitrogen.

29 Claims, 6 Drawing Sheets

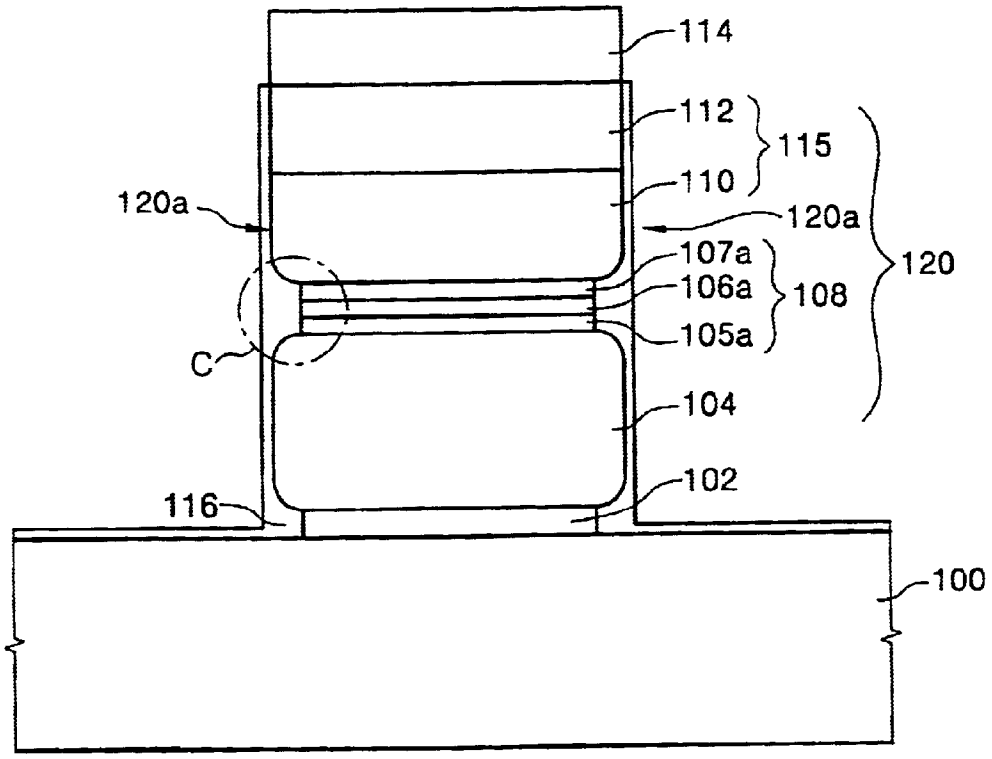


FIG.1
(PRIOR ART)

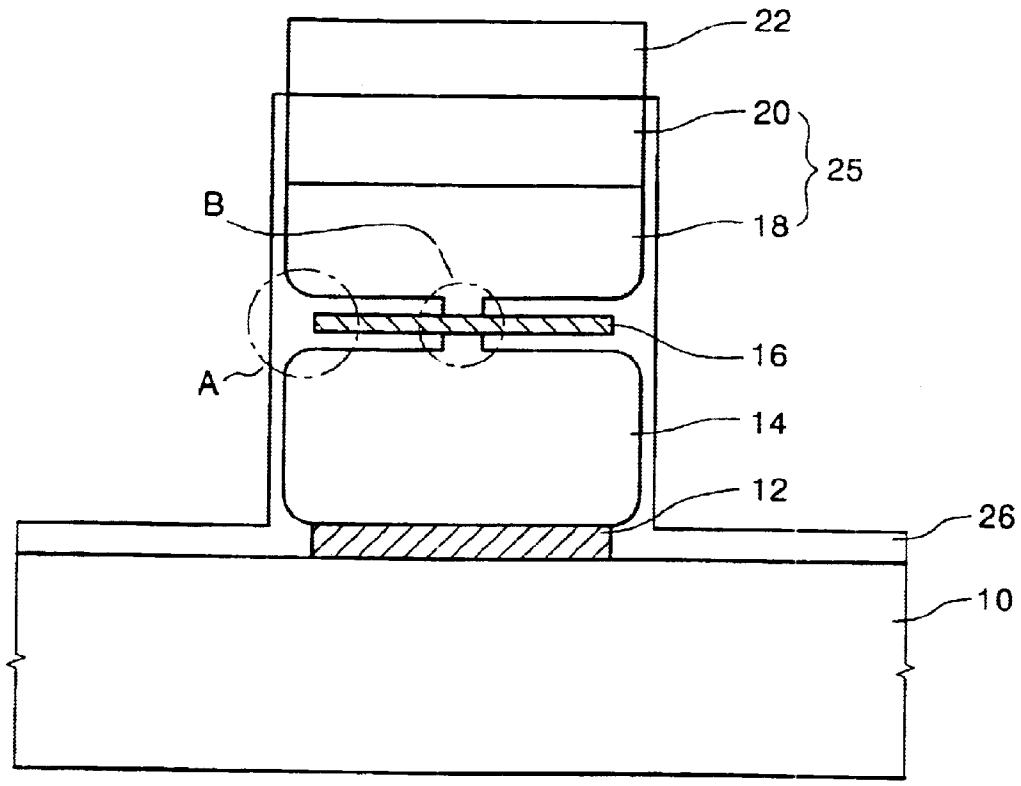


FIG.2A

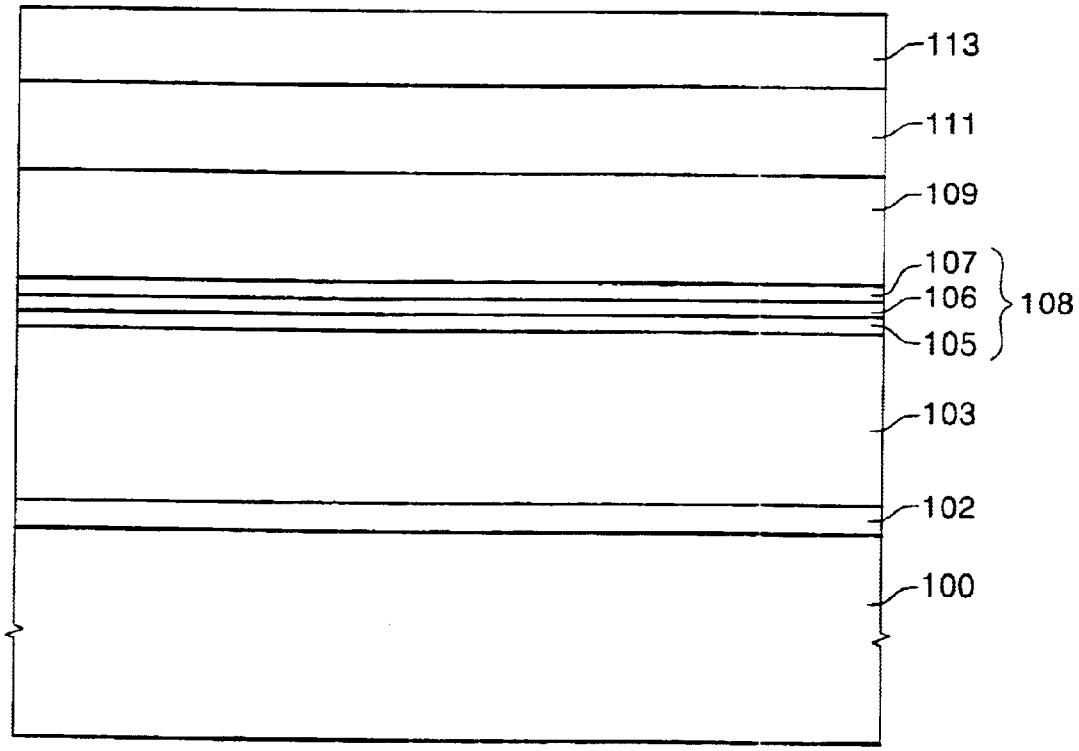


FIG.2B

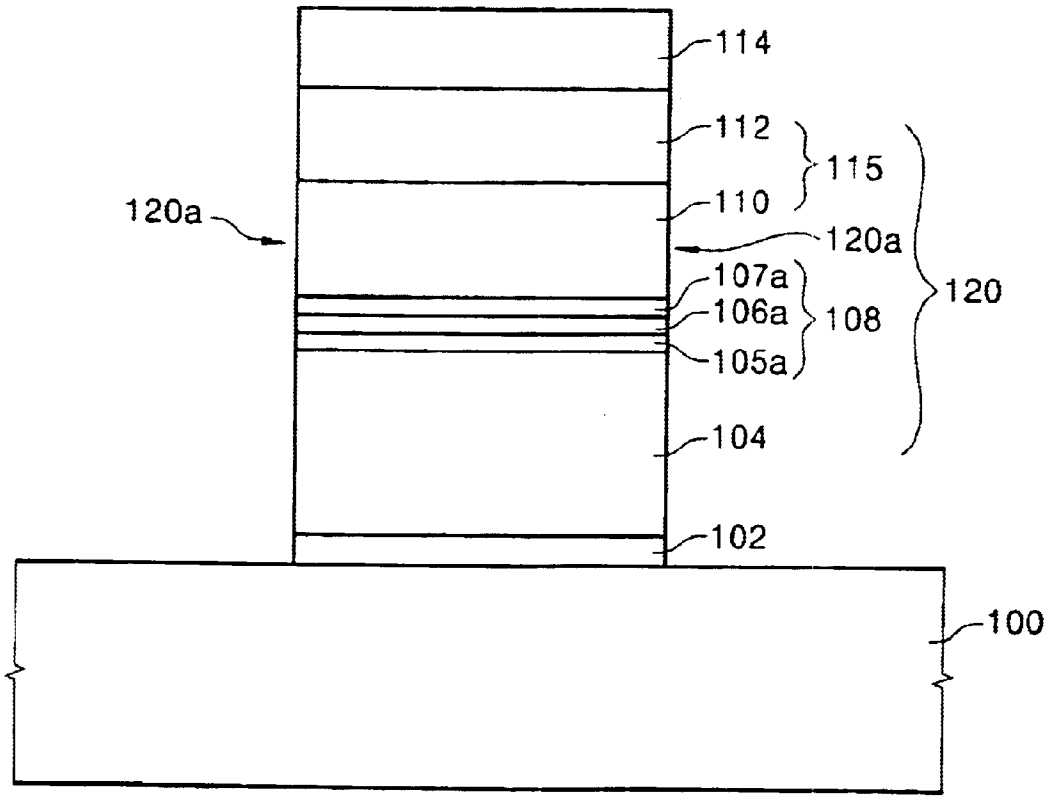


FIG.2C

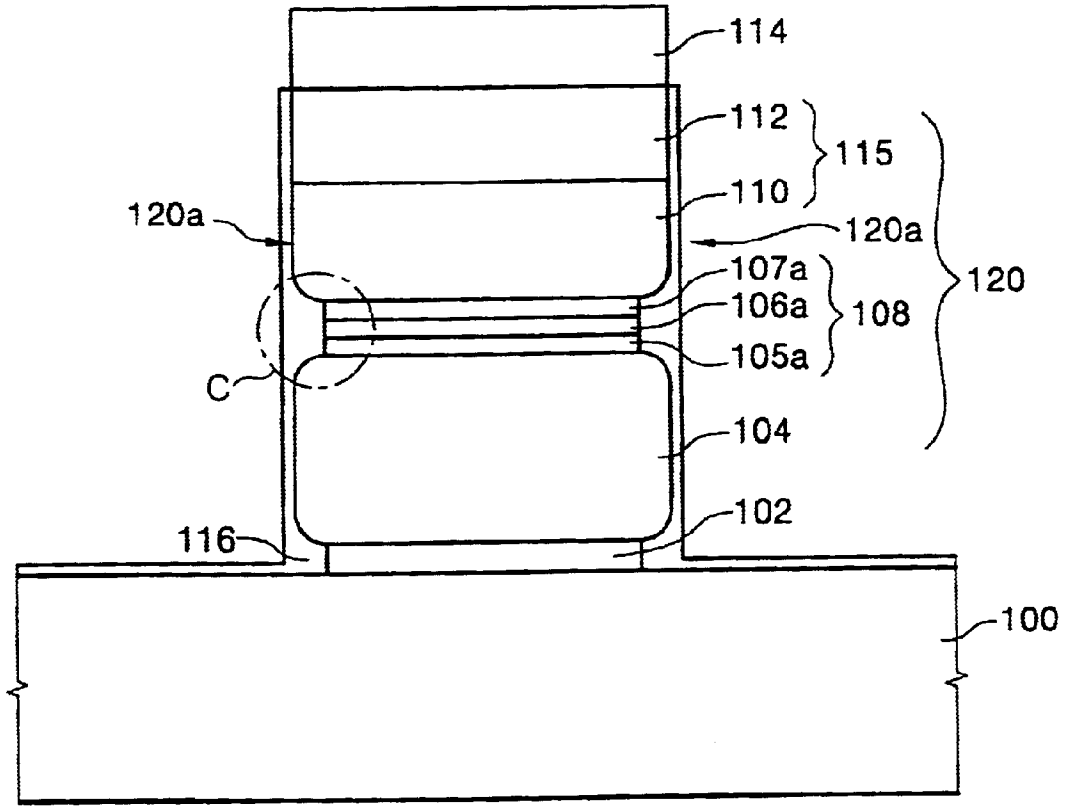

114
112
115
110
120a
120a
107a
106a
108
105a
120
C
104
102
116
100

FIG.3

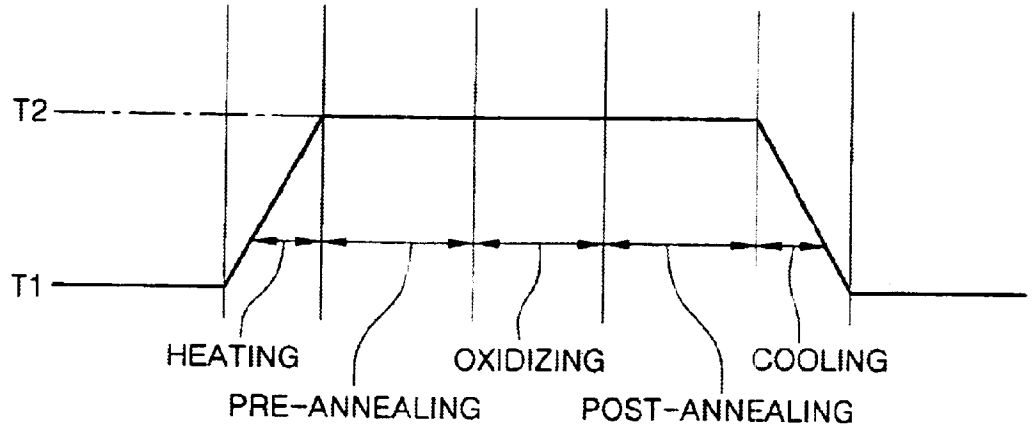
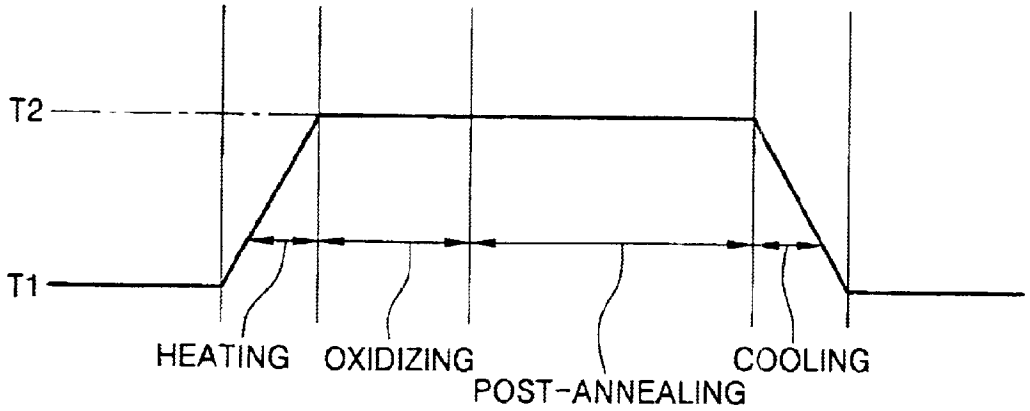

T2
T1
HEATING
PRE-ANNEALING
OXIDIZING
POST-ANNEALING
COOLING

FIG.4


T2
T1
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OXIDIZING
POST-ANNEALING
COOLING

FIG.5

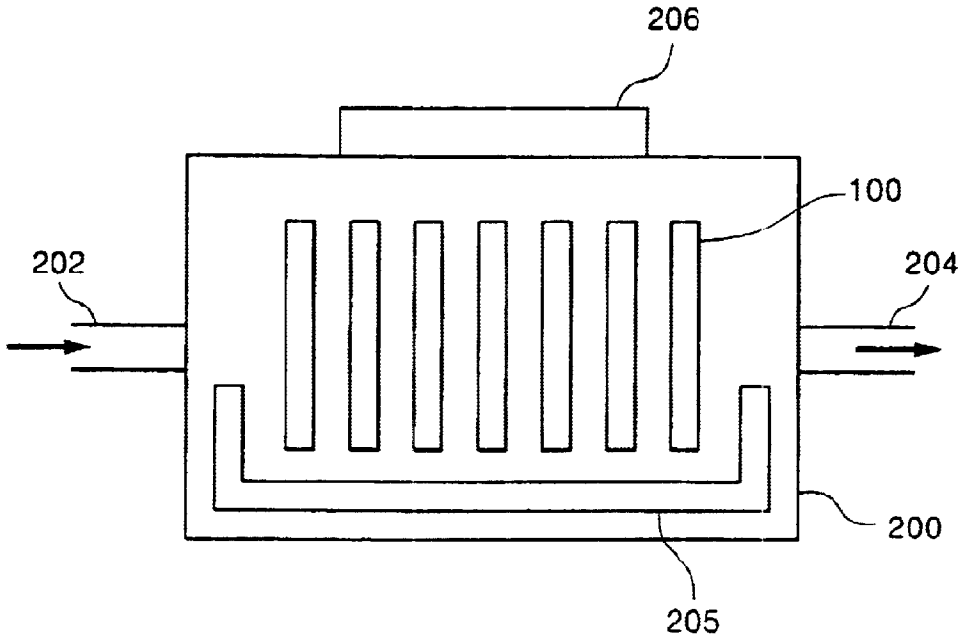
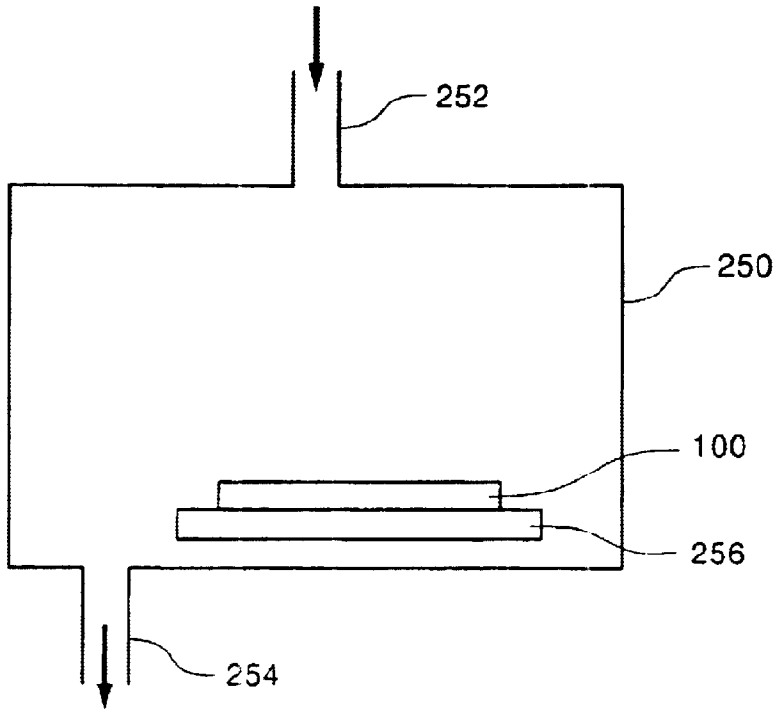


FIG.6



METHODS FOR MANUFACTURING STACKED GATES INCLUDING OXIDE/NITRIDE/OXIDE (ONO) INTERLAYER DIELECTRICS USING PRE-ANNEALING AND/OR POST-ANNEALING IN NITROGEN

RELATED APPLICATION

This application claims the benefit of Korean Patent Application No. 2002-46612, filed Aug. 7, 2002, the disclosure of which is hereby incorporated herein by reference in its entirety as if set forth fully herein.

FIELD OF THE INVENTION

This invention relates to semiconductor device manufacturing methods, and more particularly to methods of manufacturing semiconductor devices including stacked genes having oxide/nitride/oxide (ONO) interlayer dielectrics.

BACKGROUND OF THE INVENTION

Stacked gate structures including ONO interlayer dielectrics are widely used, for example, in flash memory devices, such as Electrically Erasable and Programmable Read-Only Memory (EEPROM) devices. In particular, a memory cell of an EEPROM device may include a stacked gate structure including a floating gate adjacent a silicon substrate, an ONO interlayer dielectric on the floating gate opposite the silicon substrate and a control gate on the ONO interlayer dielectric opposite the floating gate. In these flash memories, data storage may be accomplished by storing electrons in the floating gate or extracting electrons from the floating gate, while appropriate voltages are applied to the control gate and/or the substrate. The design and operation of flash memory devices such as EEPROMs are well known to those having skill in the art and need not be desired further herein.

FIG. **1** is a cross-sectional view showing a non-volatile semiconductor memory device that is fabricated according to a conventional manufacturing method.

Referring to FIG. **1**, a tunnel oxide film **12** (such as a gate oxide film) is formed in a semiconductor substrate **10**, such as a silicon semiconductor substrate, that is divided into an active region and a field region. After a first polysilicon film is coated on the tunnel oxide film, the first polysilicon film is partially removed from the field region through a photolithography process, so that the floating gates formed in adjacent active regions are electrically insulated from each other.

Then, an oxide/nitride/oxide (ONO) layer **16** is formed on the substrate **10** having the resultant structure. The ONO layer **16** serves as an interlayer dielectric, and includes a first oxide film, a nitride film, and a second oxide film.

A second polysilicon film and a metal silicide film are successively formed on the ONO layer **16**. After a hard mask layer for patterning the gate is formed on the metal silicide film, the hard mask layer is patterned to form a hard mask pattern **22**.

The metal silicide film, the second polysilicon film, the ONO layer **16**, and the first polysilicon film are successively etched using the hard mask pattern **22** as an etching mask. Thus, a stacked gate of a memory cell including a floating gate **14** and a control gate **25** with the ONO layer **16** therebetween, is formed on the substrate **10**. The floating gate **14** includes a first polysilicon pattern, and the control gate **25** includes a second polysilicon pattern **18** and a metal silicide pattern **20**.

After the patterning process for forming the stacked gate is completed, a process for oxidizing the gate sidewalls is executed in order to cure the damage to the lateral (end) portions of the ONO layer **16** and the damage to the substrate **10** under the edge portion of the floating gated **14** that may be caused by the prior etching process. The process for oxidizing the gate is conventionally performed at a temperature of more than approximately 600° C. about 3 hours. As a result, an oxide film **26** is formed on the surface of the substrate **10**, on the sidewalls of the floating gate **14**, and on the sidewalls of the control gate **25**, by an oxidation process. The oxide film **26** also can function as a buffer layer for reducing or preventing the substrate **10** from being damaged during a successive ion implantation process for forming a source/drain region.

In general, the oxide film is formed in accordance with the following reaction equation:

$$Si+O_2,\ H_2O \rightarrow SiO_2.$$

As shown the above reaction equation, oxidizing agents are diffused into a layer including silicon to produce an oxidation reaction between the silicon and the oxidizing agents. Thus, the oxidation reaction occurs at the sidewalls of the floating gate **14**, at the interface between the floating gate **14** and the ONO layer **16**, at the interface between the control gate **15** and the ONO layer **16**, and at the sidewalls of the control gate **25**.

However, the oxidizing agents may permeate from the upper portion of the control gate **25** to the central portion B of the ONO layer **16** so that a bird's beak A may occur as shown in FIG. **1**, since the oxidation process is performed at a temperature of more than 600° C. for a long time. In the same manner, the oxidizing agents may permeate from the upper portion of the floating gate **14** to the central portion B of the ONO layer **16** so that a bird's beak A further occurs. As the thickness of the ONO layer **16** increases due to the bird's beak, the capacitance between the floating and the control gates **14** and **25**, respectively, may be reduced. In addition, the programming speed and/or the cell current may be reduced. Furthermore, because the electric field may be concentrated at the portion where the ONO layer **16** is thin, dielectric breakdown of the ONO layer **16** may occur.

SUMMARY OF THE INVENTION

Some embodiments of the present invention provide methods for manufacturing a semiconductor device including a stacked gate having stacked gate sidewalls and an oxide/nitride/oxide (ONO) interlayer dielectric. According to some embodiments of the invention, pre-annealing is performed on the stacked gate in a first atmosphere comprising nitrogen. At least a portion of the stacked gate sidewalls of the stacked gate that has been pre-annealed is oxidized. Post-annealing is then performed on the stacked gate including the stacked gate sidewalls that have been oxidized, in a second atmosphere comprising nitrogen.

In other embodiments of the invention, a temperature of a batch furnace having therein a semiconductor device that includes a stacked gate having stacked gate sidewalls and an ONO interlayer dielectric, is raised in an inert gas atmosphere. Pre-annealing is performed on the stacked gate in the batch furnace in a first atmosphere that comprises nitrogen. At least a portion of the stacked gate sidewalls of the stacked gate that has been pre-annealed is oxidized. Post-annealing is performed on the stacked gate including the stacked gate sidewalls that have been oxidized, in a second atmosphere comprising nitrogen.

According to still other embodiments of the invention, a temperature of a single wafer rapid oxidation apparatus

having therein a semiconductor device that includes a stacked gate having stacked gate sidewalls and an ONO interlayer dielectric, is raised in an inert gas atmosphere. At least a portion of the stacked gate sidewalls of the stacked gate is oxidized in the single wafer rapid oxidation apparatus in which the temperature has been raised. Post-annealing then is performed on the stacked gate including the stacked gate sidewalls that have been oxidized, in an atmosphere comprising nitrogen.

In all of the above embodiments, the first and second atmospheres may comprise at least one of N_2, N_2O and NO. Moreover, in all of the above embodiments, the first and second atmospheres may comprise different gasses. Also, in all of the above embodiments, the pre-annealing, oxidizing and post-annealing may be performed at the same temperature. Finally, in all of the above embodiments, the inert gas atmosphere may comprise at least one of N_2, N_2O, NO, Ar and He.

In some embodiments, the pre-annealing, oxidizing and post-annealing are performed in a single processing chamber. In other embodiments, the pre-annealing and the oxidizing are performed in separate processing chambers. In still other embodiments, the raising, the pre-annealing, the oxidizing and the post-annealing are all performed in a batch furnace. In yet other embodiments, the oxidizing and the post-annealing are performed in a single wafer rapid oxidation apparatus. Finally, in still other embodiments, the post-annealing is performed in a batch furnace.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a non-volatile semiconductor memory device that is fabricated according to a conventional manufacturing method;

FIGS. **2**A to **2**C are cross-sectional views illustrating methods of manufacturing semiconductor devices, according to embodiments of the present invention, during intermediate fabrication steps according to embodiments of the present invention;

FIG. **3** is a graph illustrating a temperature profile according to some embodiments of the present invention;

FIG. **4** is a graph illustrating a temperature profile according to other embodiments of the present invention;

FIG. **5** is a schematic cross-sectional view of a batch furnace that may be used in embodiments of the present invention; and

FIG. **6** is a schematic cross-sectional view of a single wafer rapid oxidation apparatus that may be used in other embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

FIGS. **2**A to **2**C are cross-sectional views illustrating methods of manufacturing semiconductor devices, according to embodiments of the present invention, during intermediate fabrication steps according to embodiments of the present invention.

Referring to FIG. **2**A, a semiconductor substrate **100**, such as a silicon semiconductor substrate, is divided into an active region and a field region by an isolation process such as a shallow trench isolation (STI) method. In detail, after the semiconductor substrate **100** is etched to a predetermined depth for forming a trench, an oxide film is formed on the semiconductor substrate **100** to cover the trench formed in the semiconductor substrate **100** through a chemical vapor deposition (CVD) process. The CVD oxide film is partially removed by an etch back process and/or a chemical-mechanical polishing (CMP) process such that the CVD oxide film remains only in the trench, thereby forming a field oxide film in the trench. Other conventional isolation technologies may be used.

The field region of the semiconductor substrate **100** can be formed through a local oxidation of silicon (LOCOS) process and/or a self-aligned shallow trench isolation (SA-STI) process in which a floating gate and the active region are simultaneously formed. Other conventional technologies also may be used.

Then, a tunnel oxide film **102** (such as a gate oxide film) having, for example, thickness of about 70 Å to about 100 Å, is formed on the semiconductor substrate **100** by a thermal oxidization process. Other techniques also may be used.

A first conductive film **103** is formed on the tunnel oxide film **102** so that the first conductive film has a thickness of, for example, about 1000 Å to about 1500 Å. In a memory device, the first conductive film **103** serves as a floating gate, and includes polysilicon and/or amorphous silicon. Subsequently, the first conductive film **103** may be highly doped with N-type impurities through a $POCl_3$ diffusion process, an ion implantation process, an in-situ doping process and/or other process. When the first conductive film **103** is partially removed from the field region of the semiconductor substrate **100** through a photolithography process (described below), the floating gate formed in adjacent active regions are electrically insulated from each other.

Still referring to FIG. **2**A, in succession, an oxide/nitride/oxide (ONO) layer **108** is formed on the first conductive film **103** on the semiconductor substrate **100**. The ONO layer **108** serves as an interlayer dielectric, and includes a first oxide film **105** such as silicon oxide, a nitride film **106** such as silicon nitride, and a second oxide film **107** such as silicon oxide. The ONO layer **108** is formed using a thermal oxidization process, a CVD process and/or other conventional techniques.

A polysilicon film **109** which may be doped N-type and, in some embodiments, a metal silicide film **111**, are successively formed on the ONO layer **108**. The polysilicon film **109** serves as a second conductive film for a control gate. The metal silicide film **111** can include tungsten silicide (WSi_x), titanium silicide ($TiSi_x$), tantalum silicide ($TaSi_x$) and/or other silicides. In some embodiments, the polysilicon film **109** has a thickness of about 1000 Å, and the metal silicide film **111** has a thickness of about 100 Å to about 1500 Å.

Then, a had mask layer **113** for patterning the gate is formed on the metal silicide film **111**. The hard mask layer **113** may include single film like an oxide film or a nitride film. Also, the hard mask layer **113** can include a composite film having oxide and nitride. Other hard mask layer compositions may be used.

Referring to FIG. **2**B, a hard mask pattern **114** defining a stacked gate region of a semiconductor device is formed by patterning the hard mask layer **113** through a photolithography process. The metal silicide film **111**, the polysilicon film **109**, the ONO layer **108**, and the first conductive film **103** are successively etched using the hard mask pattern **114** as an etching mask during a dry etching process and/or other etching process. Hence, a stacked gate **120** including a floating gate **104**, a control gate **115** and an ONO interlayer dielectric **108** therebetween, is formed on the semiconductor substrate **100**. The stacked gate **120** includes stacked gate sidewalls **120***a*. The floating gate **104** includes a first conductive pattern formed by patterning the first conductive film, and the control gate **115** includes a polysilicon pattern **110** and a metal silicide pattern **112** which are formed by patterning the polysilicon film **109** and the metal silicide film **111**, respectively.

In FIG. **2**B, reference numerals of **105***a*, **106***a* and **107***a* represent a first oxide pattern, a nitride pattern, and a second oxide pattern, respectively. Thus, the ONO layer **108** includes the first oxide pattern **105***a*, the nitride pattern **106***a*, and the second oxide pattern **107***a*.

Referring to FIG. **2**C, after the patterning process for forming the stacked gate **120** is completed, a process for oxidizing the gate is executed. As a result, an oxide film having, for example, a thickness of less than approximately 40 Å, is formed on the surface of the substrate **100**, and on at least a portion of the stacked gate sidewalls **120**, for example on at least a portion of the sidewalls of the floating gate **104**, and on at least a portion of the sidewalls of the control gate **115**, in accordance with the oxidation process.

FIG. **5** is a schematic cross-sectional view illustrating a batch furnace for oxidizing a gate according to some embodiments of the present invention, and FIG. **6** is a schematic cross-sectional view illustrating a single wafer rapid oxidation apparatus for oxidizing a gate according to other embodiments of the present invention. In embodiments of the present invention, the process for oxidizing the stacked gate can be accomplished using the batch furnace and/or the single wafer rapid oxidation apparatus with various recipes.

The batch furnace of FIG. **5** can simultaneously process a plurality of wafers, and includes a chamber **200**, a carrier or a boat **205**, a gas inlet **202**, a vacuum port **204**, and a heater **206**. The boat **205** transfers the semiconductor substrates **100** such as a plurality of wafers into the chamber **200** and/or draws out the semiconductor substrates **100** from the chamber **200**. A reaction gas or other gas flows into the chamber **200** through the gas inlet **202**. The vacuum port **204** maintains the pressure of the chamber **200**, and the heater **206** also maintains the chamber **200** at a desired temperature.

The single wafer rapid oxidation apparatus can separately process the wafers, and includes a reaction chamber **250**, a substrate table **256**, a gas inlet **252**, and a vacuum port **254** as shown in FIG. **6**. The substrate **256** supports a semiconductor substrate **100** such as a wafer. The functions of the gas inlet **252** and the vacuum port **254** can be identical to those of the batch type furnace.

Hereinafter, methods for oxidizing stacked gates according to embodiments of present invention will be described.

FIG. **3** is a graph illustrating a temperature profile according to some embodiments of the present invention, which may be accomplished with a batch furnace shown in FIG. **5**, in some embodiments of the present invention. Referring to FIGS. **3** and **5**, the substrate **100** including the stacked gate **120** having the ONO layer **108** is loaded into the chamber **200** of the batch furnace.

While the chamber **200** is heated from an initial temperature T1 to a processing temperature T2, inert gases including at least one of N_2, N_2O, NO, Ar and He are introduced into the chamber **200** through the gas inlet **202** such that the growth of an oxide film is restrained on the substrate **100**. Because the substrate **100** is not significantly exposed to oxygen during the steps of loading and heating the substrate **100**, a significant bird's beak is not formed at the ends of the ONO layer **108** during a successive oxidation process.

When the temperature of the chamber **200** is raised to the processing temperature T2, for example, a temperature of more than approximately 600° C., a first atmosphere comprising nitrogen (N) flows into the chamber **200** through the gas inlet **202** so that the substrate **100** is pre-annealed. In some embodiments, the first atmosphere comprising nitrogen includes at least one of an N_2 gas, an N_2O gas and an NO gas.

Without wishing to be bound by any theory of operation, when the substrate **100** is pre-annealed with the first atmosphere comprising nitrogen, a film containing nitrogen appears to be formed on the surface of the substrate **100** and on the sidewalls **102***a* of the stacked gate **120**. Thus, bonds of Si—N having high bonding strength appear to be generated at the surface of the substrate **100** and on the sidewalls **120***a* of the stacked gate **120**, while the dangling bonds of Si appear to be reduced. These bonds of Si—N do not appear to break during the successive oxidation process so that oxidizing agents do not appear to penetrate into the central portion of the ONO layer **108**.

Continuing with the description of FIG. **3**, the oxidizing process, for example a dry oxidation process with an O_2 gas, is performed in order to cure the damage that may have occurred at the ends of the ONO layer **108**, under the processing temperature T2. Thus, as shown in FIG. **2**C, an oxide film **116** having a thickness of, for example, no more than about 40 Å, is formed on the surface of the substrate **100**, and on the sidewalls of the floating gate **104** and the control gate **115**.

Without wishing to be bound by any theory of operation, the oxidizing agents do not appear to permeate into the central portion of the ONO layer **108** due to the film containing nitrogen that was previously formed on the surface of the substrate **100** and on the sidewalls **120***a* of the stacked gate **120** during the oxidation process. Hence, the generation of the bird's beak can be reduced or minimized at the ends of the ONO layer **108** (see "C" in FIG. **2**C). Thus, the process for oxidizing the gate can be reliably performed because the damaged lateral portion of the ONO layer **108** caused by etching the gate can be oxidized, without substantial, if any, oxidation of the central portion of the ONO layer **108**.

Subsequently, the substrate **100** is post-annealed using a second atmosphere comprising nitrogen provided through the gas inlet **202** as the processing temperature T2 is maintained. The second atmosphere comprising nitrogen can include one of N_2 gas, N_2O gas, and NO gas. In some embodiments, the first and second atmospheres comprising nitrogen are the same and, in other embodiments, they are different.

Without wishing to be bound by any theory of operation, when the substrate **100** is post-annealed with the second atmosphere comprising nitrogen, nitrogen appears to be piled up at the boundaries of the oxide film **116**, the substrate **100** and the stacked gate **120** so that a silicon oxy-nitride film (SiO_xN_y) appears to be formed. The bonds of Si—N in the silicon oxy-nitride film can reduce trap sites, and can make the oxide film **116** stable under the stress caused by heat and/or electric field.

Finally, the chamber **200** is cooled from the processing temperature T2 to a lower temperature such as the initial temperature T1. The substrate **100** then is unloaded from the chamber **200** using the boat **205**.

In some embodiments of the present invention, the steps of pre-annealing the substrate **100**, forming the oxide film **116** (oxidizing), and the post-annealing the substrate **100** are performed at the processing temperature T2 corresponding to a main temperature. In some embodiments, those steps are all performed in-situ in a batch furnace or other apparatus.

FIG. **4** is a graph illustrating a temperature profile according to other embodiments of the present invention, which may be accomplished in a single wafer rapid oxidation apparatus shown in FIG. **6**.

Referring to FIGS. **4** and **6**, the substrate **100** including the stacked gate **120** having the ONO layer **108** is loaded into the chamber **250** of the single wafer oxidation apparatus. While the chamber **250** is heated from an initial temperature T1 to a processing temperature T2, an inert gas including at least one of N_2, N_2O, NO, Ar and He are introduced into the chamber **250** via the gas inlet **252** so that the growth of an oxide film is at least partially restrained on the substrate **100**. Because the substrate **100** is not significantly exposed to oxygen during the steps of loading and heating the substrate **100**, the growth of a significant bird's beak can be restrained at the lateral portion of the ONO layer **108** during a successive oxidation process.

When the temperature of the chamber **250** is raised to the processing temperature T2, for example a temperature of approximately 950° C., the oxidation process, for example a dry oxidation process using an O_2 gas, is executed for no more than approximately one minute in some embodiments and, in some embodiments approximately 40 seconds, in order to cure the damage of the lateral portion of the ONO layer **108**. Thus, an oxide film **116** having a thickness of, for example, no more than approximately 40 Å is formed on the surface of the substrate **100**, and at the sidewalls of the floating gate **104** and the control gate **115**.

In general, the time of the process can be shortened with the single wafer rapid oxidation apparatus because the single wafer rapid oxidation apparatus can more than compensate for the reduced throughput of the process compared to that of the batch type furnace by using high temperature. Hence, when using the process for oxidizing the gate for a short time using the single wafer rapid oxidation apparatus, oxidizing agents do not appear to permeate into the end portions of the ONO layer **108**, thereby reducing or minimizing the growth of the bird's beak (see "C" in FIG. **2**C).

While the chamber **250** is maintained at the processing temperature T2, an atmosphere comprising nitrogen flows into the chamber **250** through the gas inlet **252** so that the substrate **100** is post-annealed. In some embodiments, the atmosphere comprising nitrogen includes at least one of N_2 gas, N_2O gas and NO gas. When the substrate **100** is post-annealed with the atmosphere including nitrogen, a silicon oxynitride film appears to be formed at the outer surfaces of the oxide film **116**, the substrate **100**, and the stacked gate **120**, as was already described.

After the chamber **250** is cooled, for example, from the processing temperature T2 to the initial temperature T1, the substrate **100** is unloaded from the chamber **250**.

In the above-described embodiments of the present invention, the steps for forming the oxide film **116** and post-annealing the substrate **100** can be performed at the processing temperature T2 corresponding to a main temperature, and also those steps can be performed in-situ in the single wafer rapid oxidation apparatus.

In methods for oxidizing a gate in accordance with other embodiments of the present invention, after the step of pre-annealing the substrate **100** (FIG. **3**) is performed using a first atmosphere comprising nitrogen with the batch type furnace as shown in FIG. **5**, the step of oxidizing the gate using a second atmosphere comprising nitrogen, and the step of post-annealing the substrate **100** may be executed with the single wafer rapid oxidation apparatus as shown in FIG. **6**.

Also, in methods for oxidizing a gate in accordance with still other embodiments of the present invention, after the step of pre-annealing the substrate **100** and the step of oxidizing the gate (FIG. **3**) are performed using a first atmosphere comprising nitrogen in the single type wafer oxidation apparatus as shown in FIG. **5**, the step of post-annealing the substrate **100** using a second atmosphere comprising nitrogen may be executed with the batch furnace as shown in FIG. **5**. Thus, the step of post-annealing the substrate **100** can compensate for the oxide film **116** not being sufficiently transformed into a silicon oxynitride film during the step of pre-annealing the substrate **100** in the single wafer rapid oxidation apparatus.

As was described above, according to some embodiments of the present invention, the increase of thickness of an ONO layer caused by a bird's beak can be reduced or eliminated while an oxide film having adequate thickness is formed on the sidewalls of a control gate and a floating gate. Thus is, the occurrence of the bird's beak can be reduced or minimized at the ends of the ONO layer. Therefore, the cell characteristic distribution of the semiconductor device can be improved and/or the capacitance between the control and the floating gates can be increased by reducing or preventing the thickness increase in the ONO layer.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A method of manufacturing a semiconductor device including a stacked gate having stacked gate sidewalls and an Oxide/Nitride/Oxide (ONO) interlayer dielectric, the method comprising:

pre-annealing the stacked gate in a first atmosphere comprising nitrogen;

oxidizing at least a portion of the stacked gate sidewalls of the stacked gate that has been pre-annealed; and

post-annealing the stacked gate including the stacked gate sidewalls that have been oxidized, in a second atmosphere comprising nitrogen.

2. A method according to claim **1** wherein the first and second atmospheres comprise at least one of N_2, N_2O and NO.

3. A method according to claim **1** wherein the first and second atmospheres comprise different gasses.

4. A method according to claim **1** wherein the pre-annealing, oxidizing and post-annealing are performed at same temperature.

5. A method according to claim 1 wherein the pre-annealing is preceded by:

raising the temperature to a pre-annealing temperature in an inert gas atmosphere.

6. A method according to claim 5 wherein the inert gas atmosphere comprises at least one of N_2, N_2O, NO, Ar and He.

7. A method according to claim 1 wherein the pre-annealing, oxidizing and post-annealing are performed in a single processing chamber.

8. A method according to claim 1 wherein the pre-annealing and the oxidizing are performed in separate processing chambers.

9. A method according to claim 1 wherein the first atmosphere is free of reactive oxygen.

10. A method according to claim 1 wherein the pre-annealing comprises pre-annealing without oxidizing.

11. A method of manufacturing a semiconductor device including a stacked gate having stacked gate sidewalls and an Oxide/Nitride/Oxide (ONO) interlayer dielectric, the method comprising:

raising a temperature of a batch furnace having the semiconductor device therein in an inert gas atmosphere;

pre-annealing the stacked gate in the batch furnace in a first atmosphere comprising nitrogen;

oxidizing at least a portion of the stacked gate sidewalls of the stacked gate that has been pre-annealed; and

post-annealing the stacked gate including the stacked gate sidewalls that have been oxidized, in a second atmosphere comprising nitrogen.

12. A method according to claim 11 wherein the first and second atmospheres comprises at least one of N_2, N_2O and NO.

13. A method according to claim 11 wherein the first and second atmospheres comprise different gasses.

14. A method according to claim 11 wherein the pre-annealing, oxidizing and post-annealing are performed at same temperature.

15. A method according to claim 11 wherein the raising, the pre-annealing, the oxidizing and the post-annealing are all performed in the batch furnace.

16. A method according to claim 11 wherein the oxidizing and the post-annealing are performed in a single wafer rapid oxidation apparatus.

17. A method according to claim 11 wherein the inert gas atmosphere comprises at least one of N_2, N_2O, NO, Ar and He.

18. A method according to claim 11 wherein the first atmosphere is free of reactive oxygen.

19. A method according to claim 11 wherein the pre-annealing comprises pre-annealing without oxidizing.

20. A method of manufacturing a semiconductor device including a stacked gate having stacked gate sidewalls and an Oxide/Nitride/Oxide (ONO) interlayer dielectric, the method comprising:

raising a temperature of a single wafer rapid oxidation apparatus having the semiconductor device therein in an inert gas atmosphere;

oxidizing at least a portion of the stacked gate sidewalls in the single wafer rapid oxidation apparatus in which the temperature has been raised; and

post-annealing the stacked gate including the stacked gate sidewalls that have been oxidized, in an atmosphere comprising nitrogen.

21. A method according to claim 20 wherein the inert gas atmosphere comprises at least one of N_2, N_2O, NO, Ar and He.

22. A method according to claim 20 wherein the atmosphere comprising nitrogen comprising at least one of N_2, N_2O and NO.

23. A method according to claim 20 wherein the oxidizing and post-annealing are performed at same temperature.

24. A method according to claim 20 wherein the atmosphere comprising nitrogen is a first atmosphere comprising nitrogen and wherein the following is performed between the raising and the oxidizing:

pre-annealing the stacked gate in the single wafer rapid oxidation apparatus in a second atmosphere comprising nitrogen.

25. A method according to claim 24 wherein the second atmosphere comprising nitrogen comprises at least one of N_2, N_2O and NO.

26. A method according to claim 24 wherein the pre-annealing and the post-annealing are both performed in the single wafer rapid oxidation apparatus.

27. A method according to claim 24 wherein the pre-annealing comprises pre-annealing without oxidizing.

28. A method according to claim 20 wherein the post-annealing is performed in a batch furnace.

29. A method according to claim 20 wherein the inert gas atmosphere is free of reactive oxygen.

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US 20050110102A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2005/0110102 A1

Wang et al. (43) Pub. Date: May 26, 2005

(54) METHOD FOR FORMING OXIDE ON ONO STRUCTURE

(75) Inventors: **Chih-Hao Wang**, Taoyuan City (TW); **Hsin-Huei Chen**, Miaoli (TW); **Chong-Jen Huang**, Taipei County (TW); **Kuang-Wen Liu**, Nantou (TW); **Jia-Rong Chiou**, Keelung (TW); **Chong-Mu Chen**, Taichung (TW)

Correspondence Address:
HAYNES BEFFEL & WOLFELD LLP
P O BOX 366
HALF MOON BAY, CA 94019 (US)

(73) Assignee: **Macronix International Co., Ltd.**, Hsin-chu (CN)

(21) Appl. No.: **10/721,605**

(22) Filed: **Nov. 25, 2003**

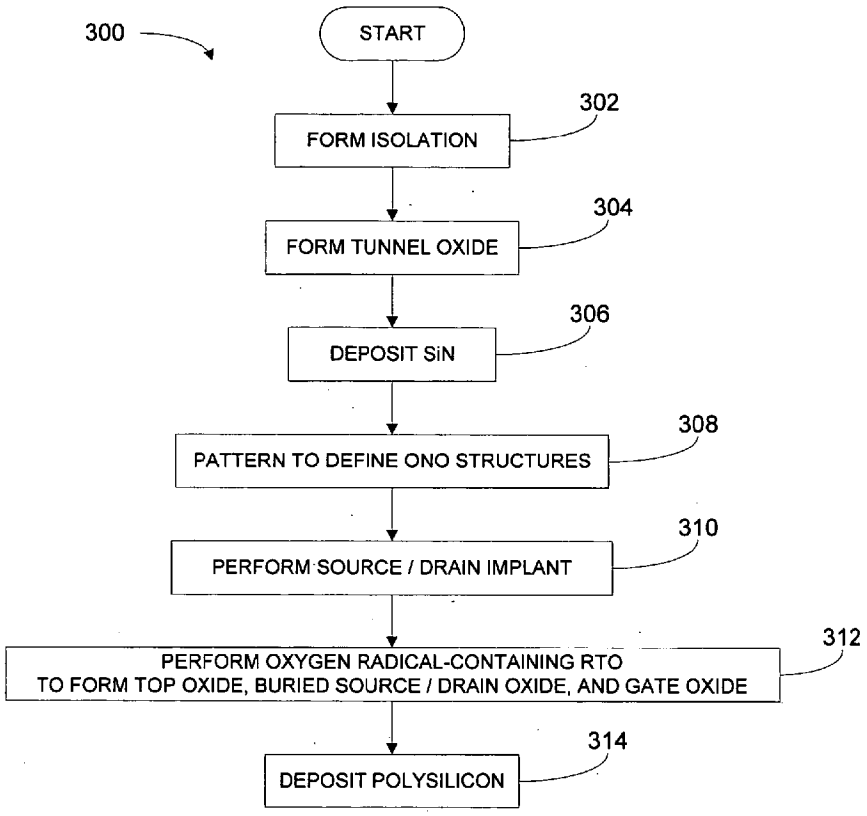
Publication Classification

(51) **Int. Cl.**[7] **H01L 29/76**

(52) **U.S. Cl.** **257/411**

(57) **ABSTRACT**

A semiconductor device having a silicon oxide/silicon nitride/silicon oxide ("ONO") structure is formed by providing a first silicon oxide layer and a silicon nitride layer over a substrate having a memory region and a logic device region; patterning the first silicon oxide layer and the silicon nitride layer to define bottom oxide and silicon nitride portions of partially completed ONO stacks and to expose the substrate in the logic device regions; performing a rapid thermal annealing process in the presence of a radical oxidizing agent to form concurrently a second silicon oxide layer on the exposed surface of the silicon nitride layer and a gate oxide layer over the substrate; and depositing a conductive layer over the completed ONO stacks and the gate oxide. The invention is employed in manufacture of, for example, memory devices having and peripheral logic devices and memory cells including ONO structures. Exposing the patterned silicon nitride to the oxygen radical during the RTO according to the invention significantly reduces the processing time, and reduces the thermal budget. Moreover, because according to the invention the upper surface and the sidewalls of the silicon nitride layer are covered by the top oxide layer, the silicon nitride is not exposed during a subsequent cleaning process. As a result of increased contact area between the polysilicon gate and the top oxide layer, the coupling ratio of the gate is increased.



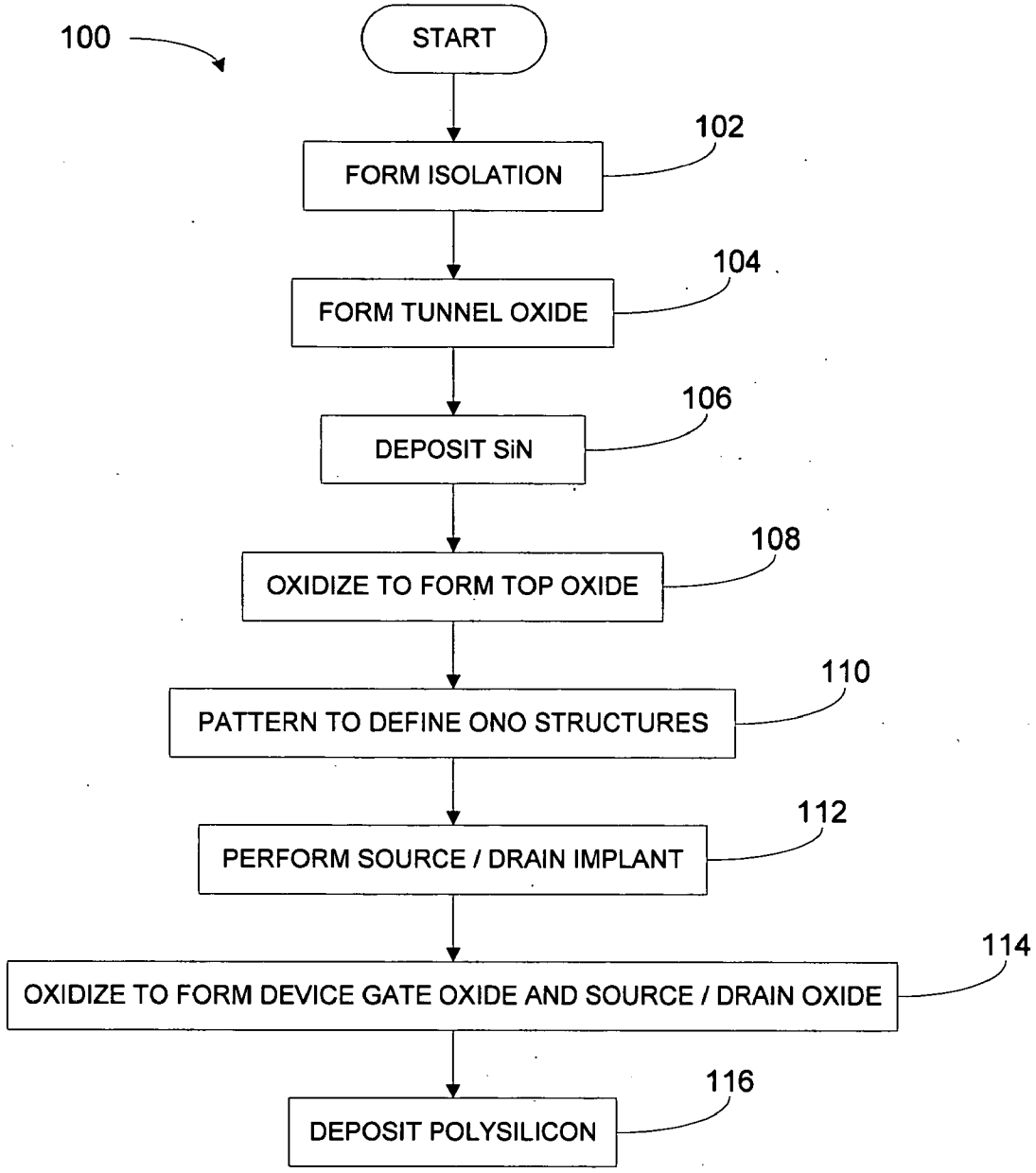


Fig. 1 (prior art)

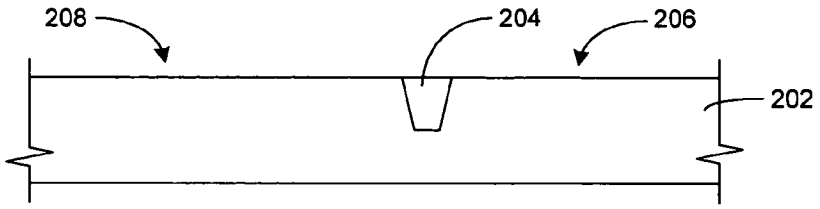


Fig. 2A (prior art)

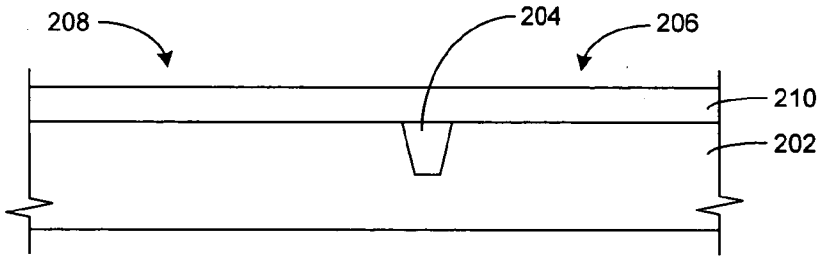


Fig. 2B (prior art)

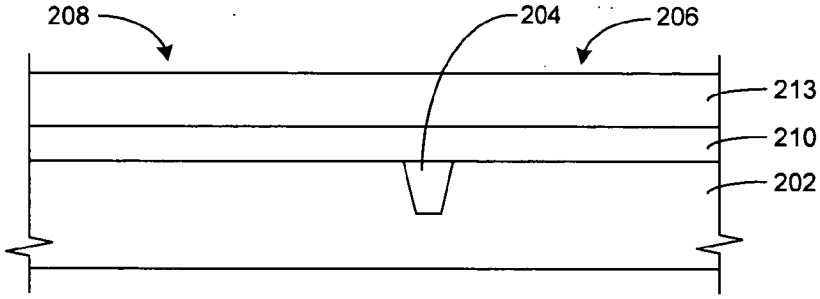


Fig. 2C (prior art)

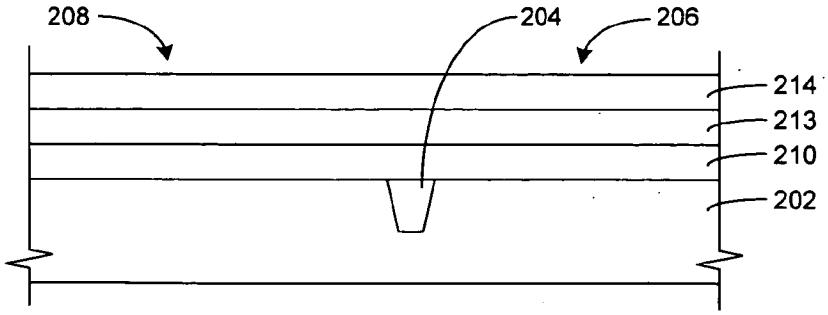


Fig. 2D (prior art)

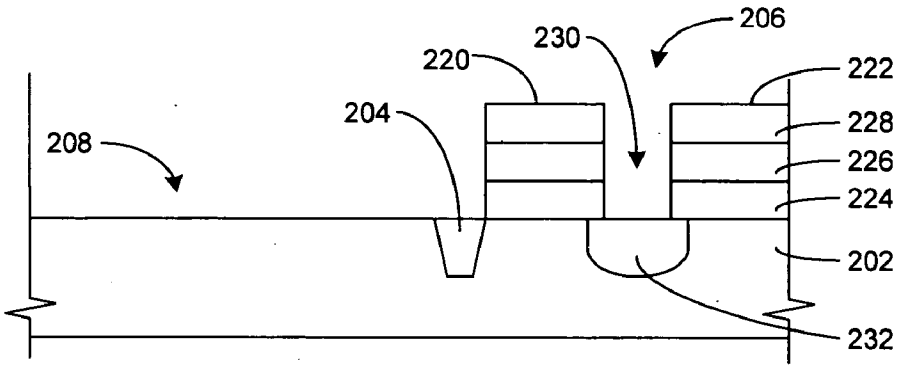


Fig. 2E (prior art)

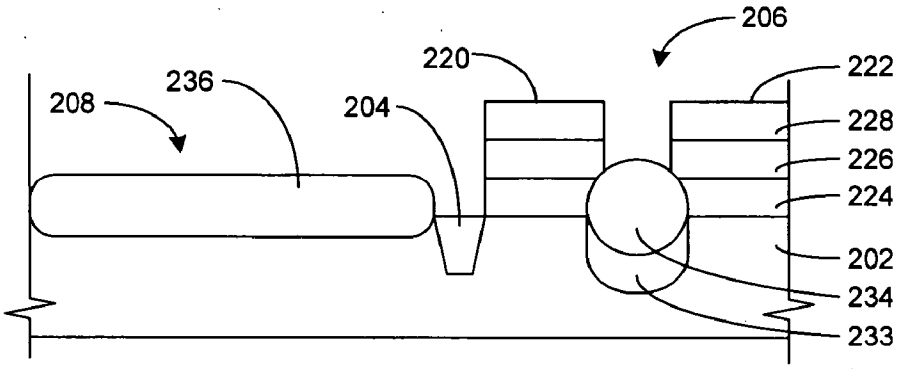


Fig. 2F (prior art)

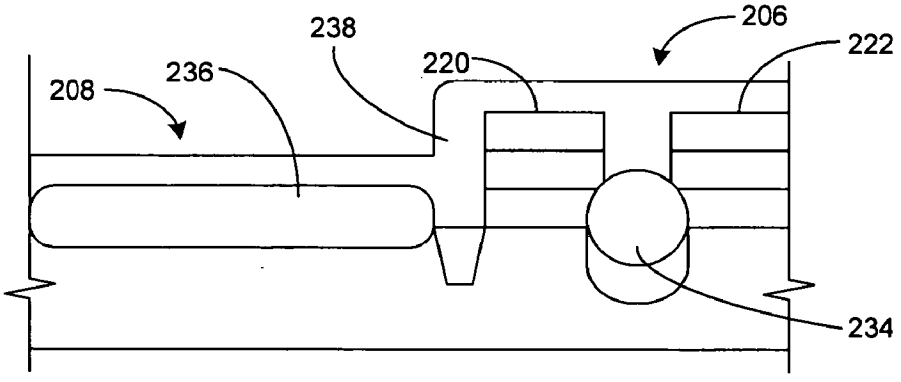


Fig. 2G (prior art)

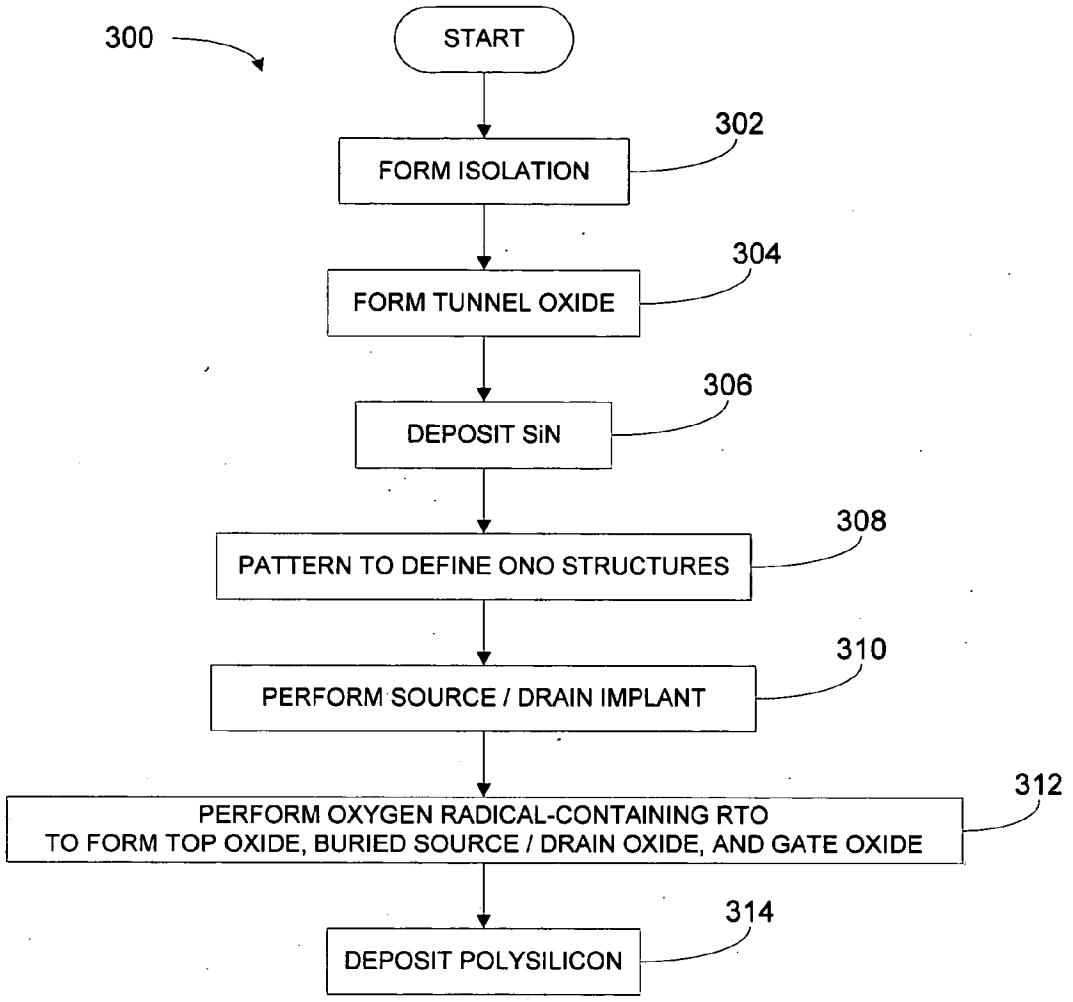

300
START
302
FORM ISOLATION
304
FORM TUNNEL OXIDE
306
DEPOSIT SiN
308
PATTERN TO DEFINE ONO STRUCTURES
310
PERFORM SOURCE / DRAIN IMPLANT
312
PERFORM OXYGEN RADICAL-CONTAINING RTO
TO FORM TOP OXIDE, BURIED SOURCE / DRAIN OXIDE, AND GATE OXIDE
314
DEPOSIT POLYSILICON

Fig. 3

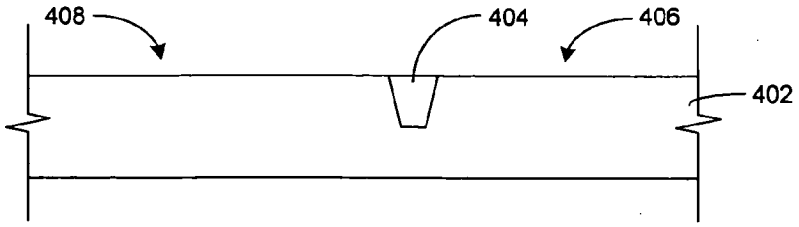


Fig. 4A

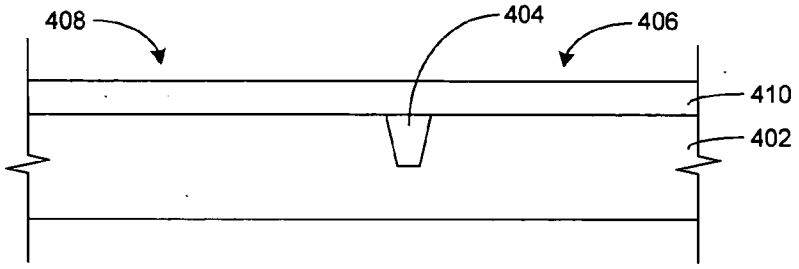


Fig. 4B

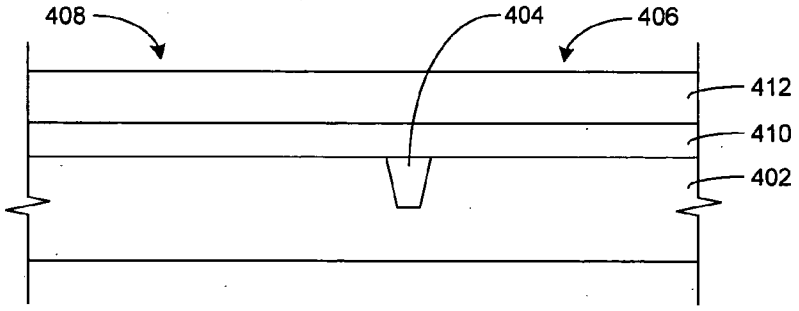


Fig. 4C

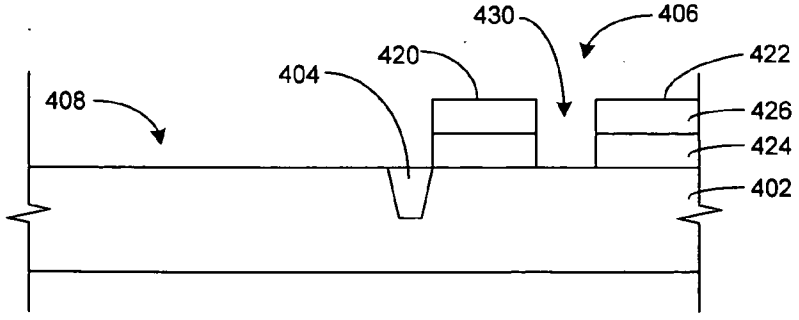


Fig. 4D

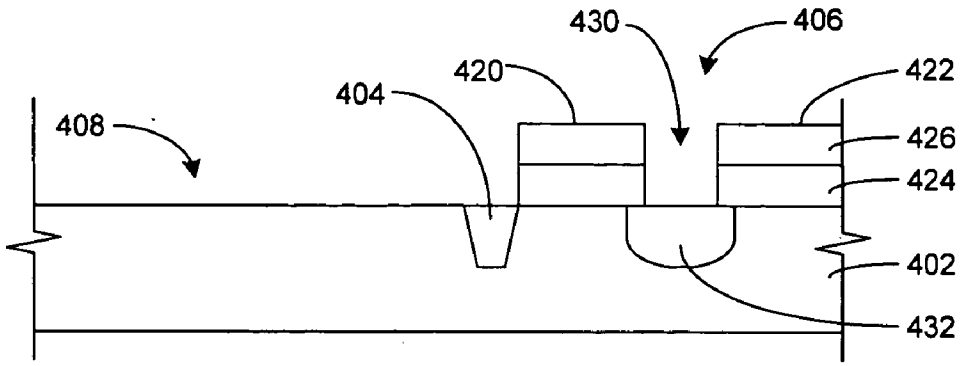


Fig. 4E

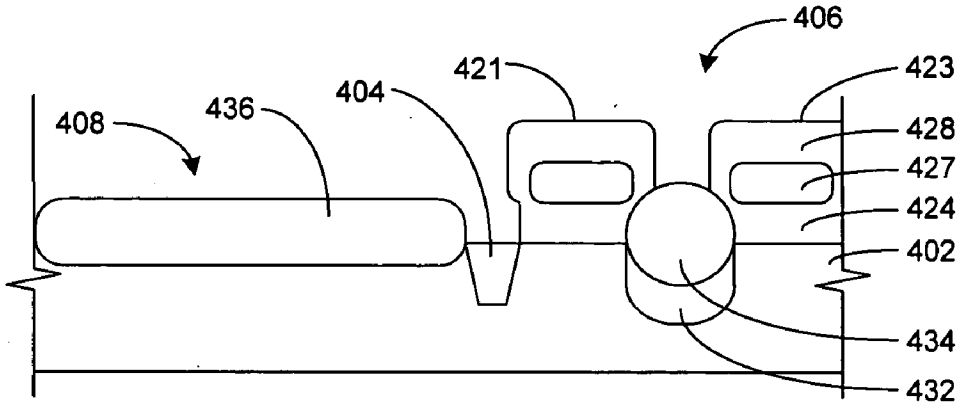


Fig. 4F

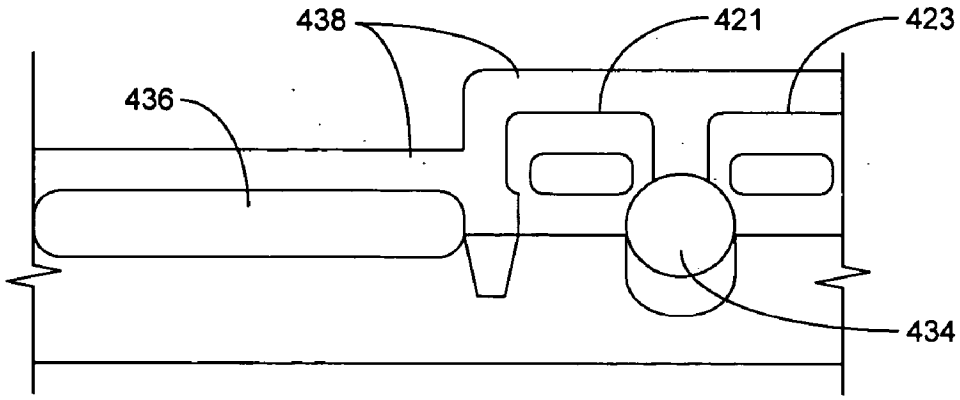


Fig. 4G

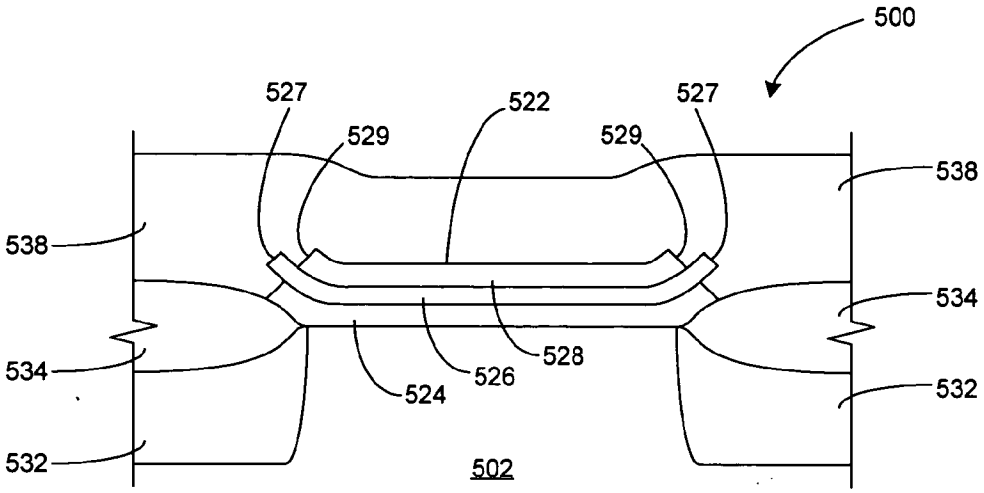

500
527
522
527
529
529
538
538
534
534
528
526
524
532
532
502

Fig. 5

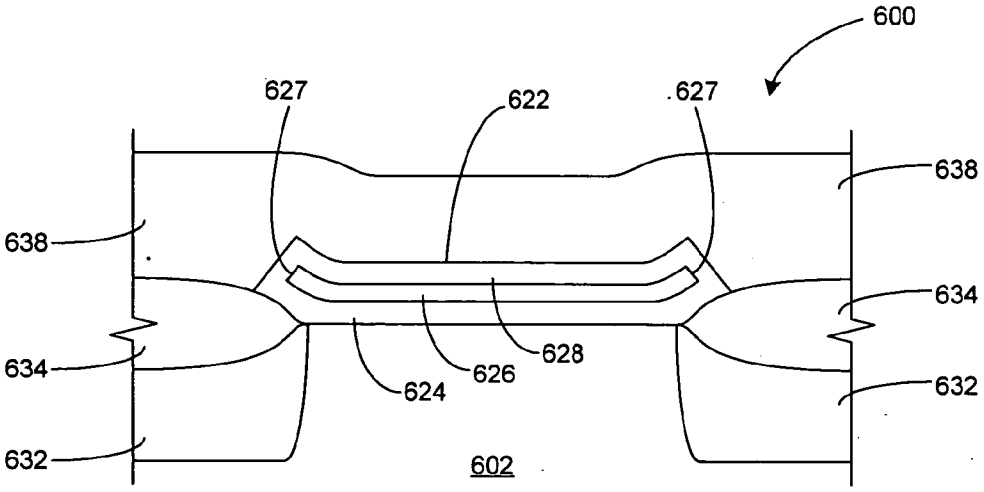

600
627
622
627
638
638
634
634
628
626
624
632
632
602

Fig. 6

METHOD FOR FORMING OXIDE ON ONO STRUCTURE

BACKGROUND

[0001] This invention relates to semiconductor devices that include a silicon oxide/silicon nitride/silicon oxide (ONO) structure, and to methods for oxide formation in such devices.

[0002] In a conventional process for making a device having an ONO structure, a tunnel layer, a silicon nitride layer and a top oxide layer are formed over a substrate, and then an etching process is performed for patterning the ONO structure.

[0003] The top oxide layer can be formed by oxidation of the silicon nitride. However, in conventional processes oxidation of silicon nitride is time-consuming and has a very high thermal budget. In some conventional processes, for example, silicon nitride is oxidized by wet oxidation within a furnace at a temperature of 1000° C. over a time period as long as 60 minutes.

[0004] Moreover, the oxidation step in such a conventional process is followed by a cleaning process, which may etch the top oxide layer, even to the extent of exposing the corners of the silicon nitride layer so as to cause a leak from the silicon nitride layer to a polysilicon gate formed subsequently. As a result, the charges stored in the silicon nitride layer will be lost, causing an electrical defect in the device.

[0005] In one conventional approach to avoiding loss of the top oxide layer during the cleaning process, a tunnel oxide layer and a silicon nitride layer are first deposited and patterned, and then a top oxide layer is grown on the silicon nitride by wet oxidation. However, the oxidation selectivity of wet oxidation for the substrate and the silicon nitride layer is relatively high, that is, the oxidation rate of wet oxidation for the substrate is far greater than that of the silicon nitride layer. Using a wet oxidation in this manner to form a 100 Å thick top oxide layer, for example, will result in a 1000 Å thick oxide layer formed on the substrate. Consequently, where a conventional wet oxidation is used, it is necessary to remove the thicker oxide layer formed on the substrate. This makes for a more complicated process, and can result in an uneven substrate surface.

[0006] One approach to growing an oxide on a substrate is referred to as the in situ steam generation ("ISSG") process. In the "ISSG" process, the substrate (typically a semiconductor wafer) is heated to a temperature high enough to catalyze a reaction between an oxygen-containing gas and a hydrogen-containing gas to form oxygen radical. Then the reactive oxygen radical can effectively oxidize the silicon or silicon nitride on the substrate.

[0007] U.S. Pat. No. 6,184,155 describes a two step ISSG process for growing an ultra-thin silicon dioxide gate insulator layer for narrow channel length MOSFET devices. A first steam oxidation and in situ anneal in a nitrous oxide ambient is followed by a second steam oxidation and in situ anneal in a nitrous oxide ambient. The two-step procedure is said to result in a silicon dioxide layer having thickness between about 10 Å and 20 Å, providing a gate insulator having reduced leakage current during standby or operating modes, as compared with silicon dioxide gate insulators formed by procedures not employing two-step ISSG.

[0008] U.S. Pat. No. 6,171,911 describes a process for selectively and sequentially forming two different thicknesses of thermally grown silicon oxide in a MOSFET device. Regions on the wafer are defined by field isolation. Conventional oxidation methods for making a gate oxide are used to grow a thicker oxide on all the exposed regions; then the wafer is masked and the mask is patterned to expose regions that are to receive a thinner oxide, and the thicker oxide is removed from those regions by wet etching using hydrofluoric acid; then the mask is stripped and the wafer is cleaned with an aqueous solution free of hydrofluoric acid. Then the wafer is subjected to a low pressure rapid thermal anneal (600° C. to 1050° C.) in an ambient containing hydrogen and nitrogen to remove native oxide and to passivate the silicon surface, reducing the residual oxide thickness to about 4 Å. This is said to result in improved thickness uniformity and oxide quality, and the residual oxide film following annealing is said to become a more robust form of silicon oxide.

SUMMARY

[0009] According to the invention, a tunnel oxide layer and a silicon nitride layer are formed and patterned, and then an in situ steam generation ("ISSG") is carried out in the presence of an oxygen radical to form simultaneously (concurrently) a top oxide layer, a buried drain oxide layer, and a gate oxide layer in the MOS region. Exposing the exposed patterned silicon nitride to the oxygen radical according to the invention can require as little as about 1 minute's time for oxidation of the silicon nitride. The process time is accordingly much shortened, and the thermal budget is reduced. Moreover, because according to the invention the upper surface and the sidewalls of the silicon nitride layer are covered by the top oxide layer, the silicon nitride is not exposed during a subsequent cleaning process. As a result of increased contact area between the polysilicon gate and the top oxide layer, the coupling ratio of the gate is also increased.

[0010] In one general aspect, the invention features a method for forming an oxide in a semiconductor device having an ONO structure, by depositing a tunnel oxide layer and a silicon nitride layer over a substrate, and patterning using a photolithographic process; and performing a rapid thermal oxide process in an oxygen radical-containing ambient to form a top oxide layer concurrently (simultaneously) on the upper surface and sidewalls of the patterned silicon nitride layer, a buried diffusion (source/drain) located in the substrate, and a gate oxide layer on the MOS region of the substrate.

[0011] An oxygen radical, as that term is used herein, is an oxygen-containing species capable of independent existence that contains one or more unpaired electrons. An unpaired electron is one that occupies an atomic or molecular orbital by itself. The oxygen radical is a strong oxidizing agent, providing for rapid oxidation of the silicon nitride. Because the difference is small between the oxidation rate for the substrate and the oxidation rate for the silicon nitride layer, oxygen selectivity for the substrate and the silicon nitride layer is low.

[0012] According to the invention, the top oxide layer, the buried drain oxide layer and the MOS gate oxide layer can be formed concurrently rather than in separate steps, sim-

plifying the process, and reducing the process time and thermal budget for the process.

[0013] In another general aspect the invention features a method for forming a semiconductor device having a silicon oxide/silicon nitride/silicon oxide ("ONO") structure, by forming a first silicon oxide layer and a silicon nitride layer over a substrate, patterning the first silicon oxide layer and the silicon nitride layer, performing a rapid thermal annealing process in the presence of a radical oxidizing agent to form concurrently (simultaneously) a second silicon oxide layer on the exposed surface of the silicon nitride layer and a gate oxide layer over the substrate.

[0014] In another general aspect the invention features a method for manufacturing a memory device having a silicon oxide/silicon nitride/silicon oxide ("ONO") structure, by forming a first oxide layer and a silicon nitride layer over a substrate having a memory region and a metal oxide semiconductor region; patterning the first oxide layer and the silicon nitride layer to form patterned first oxide layers and patterned silicon nitride layers on the memory cell region; forming buried source/drains in the regions of the substrate between the patterned first oxide layers; performing a rapid thermal annealing process in the presence of a radical oxidizing agent, concurrently (simultaneously) forming a second silicon oxide layer on the exposed surface of the patterned silicon nitride layer, buried drain oxide layers on the buried source/drains, and a gate oxide layer on the metal oxide semiconductor region.

[0015] In some embodiments the radical oxidizing agent includes an oxygen radical, and in particular embodiments the oxygen radical is O.

[0016] In some embodiments the ratio of the thicknesses of the resulting second silicon oxide layer and gate oxide layer is in the range about 0.6:1 to about 0.8:1. In some embodiments, where the device is a memory device having buried source/drains, the thickness of the resulting buried drain oxide layer is greater than the thickness of the resulting gate oxide layer.

[0017] In some embodiments the rapid thermal annealing process is an in situ steam generation process, in which the temperature of the substrate (typically a semiconductor wafer) is heated to a temperature within a suitable range, and a hydrogen-containing gas and an oxygen-containing gas are introduced at flow rates within a suitable range, for a period of time suitable to complete the oxidation process. In some embodiments the hydrogen-containing gas and the oxygen-containing gas are introduced together with and in a proportion to a carrier gas within a suitable range.

[0018] In some embodiments the hydrogen-containing gas is H_2 and the oxygen-containing gas is O_2, and the carrier gas (if employed) is N_2; the H_2 and O_2 are introduced at flow rates proportionately in a range (H_2/H_2+O_2) about 0.1% to about 40%, more usually in a range about 5% to about 33% (H_2/H_2+O_2), and in particular embodiments at flow rates proportionately about 1:19 or 1:3 or 1:2 (H_2: O_2); the wafer is held at a temperature in a range about 700° C. to about 1300° C., more usually in a range about 900° C. to about 1150° C. The wafer is exposed to the gas mixture for a time, depending upon the oxide thicknesses desired and depending upon the gas flow rates and the temperature, as few as 1 to 10 seconds and as long as 100 to 1000 seconds or more, more usually for a time as few as 10 seconds, and in particular embodiments for a time as few as 30 seconds, and in some embodiments as long as 120 seconds, and in other embodiments as long as 300 seconds, and in still other embodiments as long as 500 seconds. In particular embodiments of the invention, a temperature of 850° C., or 900° C., or 950° C., or 1000° C. is used; and hydrogen and oxygen are flowed at a ratio (H_2/H_2+O_2) about 5%, or 25%, or 33% (e.g., H_2 at 6 slm and O_2 at 12 slm) for a process time about 30 seconds, or 60 seconds, or 90 seconds, or 120 seconds.

[0019] In another general aspect the invention features a semiconductor device having a silicon oxide/silicon nitride/silicon oxide structure, including a first silicon oxide layer over a substrate; a silicon nitride layer over a portion of the first silicon oxide layer; a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer; and a gate conducting layer over the silicon oxide layer.

[0020] In another general aspect the invention features a memory cell having a silicon oxide/silicon nitride/silicon oxide structure, including a buried drain and source located within a substrate; a buried drain/source oxide layer over the buried drain/source; a first silicon oxide layer covering a region of the substrate located between the buried drain/source and covering a portion of the buried drain/source oxide layer; a silicon nitride layer covering a portion of the first silicon oxide layer; a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer; and a gate conducting layer over the second silicon oxide layer.

[0021] In another general aspect the invention features a memory cell having a silicon oxide/silicon nitride/silicon oxide structure in a non-volatile memory, including a buried drain and source located within a substrate; a buried drain/source oxide layer over the buried drain/source; a first silicon oxide layer covering a region of the substrate located between the buried drain and the buried source and covering a portion of the buried drain/source oxide layer; a silicon nitride layer covering a portion of the first silicon oxide layer; a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer; and a gate conducting layer over the second silicon oxide layer.

[0022] In some embodiments the ratio of the thicknesses of the oxide layers on the SiN and on the Si is in a range (SiN/Si) about 0.6:1 to 0.8:1, more usually in a range about 0.68:1 to 0.78:1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] **FIG. 1** is a flow diagram showing steps in a conventional oxide forming process.

[0024] **FIGS. 2A-2G** are diagrammatic sketches in sectional view showing stages in a conventional oxide forming process as in **FIG. 1**.

[0025] **FIG. 3** is a flow diagram showing an oxide forming process according an embodiment of the invention.

[0026] **FIGS. 4A-4G** are diagrammatic sketches in sectional view showing stages in an oxide forming process according to an embodiment of the invention as in **FIG. 3**.

[0027] **FIG. 5** is a diagrammatic sketch in a sectional view of an ONO structure formed according to a conventional process.

[0028] **FIG. 6** is a diagrammatic sketch in a sectional view showing an ONO structure formed according to the invention.

DETAILED DESCRIPTION

[0029] The invention will now be described in further detail by reference to the drawings, which illustrate alternative embodiments of the invention. The drawings are diagrammatic, showing features of the invention and their relation to other features and structures, and are not made to scale. For improved clarity of presentation, in the Figs. illustrating embodiments of the invention, elements corresponding to elements shown in other drawings are not all particularly renumbered, although they are all readily identifiable in all the Figs.

[0030] According to illustrative embodiments of the invention the oxygen radical is formed in situ, that is, at the heated wafer surface by reactions of H_2 and O_2 under ISSG conditions. The in situ steam generation process is a low-pressure process wherein H_2 and O_2 are proportionately mixed and are introduced into the process chamber directly, without pre-combustion. The wafer is heated, and the reaction between H_2 and O_2 occurs near the wafer surface ("in situ") because the hot wafer acts as the ignition source. Generally, under ISSG conditions the oxygen radical **00** is created primarily by way of the following reactions:

$H_2+O_2 \rightarrow 2OH$

$H_2+OH \rightarrow H_2O+H$

$O_2+H \rightarrow OH+O.$

$H_2+O\ OH+H$

[0031] The presence of hydrogen during ISSG oxidation accelerates dissociation of molecular oxygen into reactive oxygen atoms. According to the invention, the rate of oxide growth on silicon nitride in the ISSG (that is, thickness of grown oxide versus thickness of silicon nitride consumed) exhibits a strong correlation with atomic oxygen (oxygen radical O.) concentration, and not to any other atomic or molecular species. The oxygen radical O. concentration is not dependent upon reactor volume, but depends upon pressure, temperature, and relative amount of hydrogen in the chamber.

[0032] The oxygen radical peak concentration results from a balance of radical generation through molecular collisions that are strong functions of temperature and pressure, and recombination processes that are strong functions of pressure or flow rate in the chamber. Accordingly, the ISSG process depends upon using process pressure, flow rate and temperature in the chamber within specified ranges. Accordingly, in some embodiments the following parameters can be effective: temperature in the range about 800° C. to about 1000° C.; pressure in the range about 1 torr to about 20 torr; flow rate of H_2+O_2 in the range about 1 slm to about 40 slm. The ratio of H_2/H_2+O_2 is in the range about 0.1% to about 40%.

[0033] In some embodiments a carrier gas such as nitrogen is flowed through the chamber along with the H_2 and O_2 mixture, and this may improve process uniformity; but the use of a carrier gas is not essential to in situ generation of the oxygen radical O. Nitrogen is introduced at a flow rate in the range 0 slm (if not used) to about 50 slm.

[0034] In a conventional process, using a high ratio of hydrogen to oxygen (such as 1/67:1) and a high temperature (such as 1000° C.) the ratio of rates of growth of oxide on nitride and on silicon (SiN/Si) as typically about 0.26. According to the invention, a much higher growth rate ratio (SiN/Si) can be achieved, and simultaneous (concurrent) oxide growth on both surfaces can be achieved.

[0035] Referring now to **FIG. 1**, a flow diagram is shown of a conventional process **100** for oxide formation in a device containing an ONO structure. Resulting structures at various stages in the conventional process are shown in diagrammatic sectional views in **FIGS. 2A through 2G**. In a step **102** of the conventional process **100**, a first region **206** and a second region **208** are defined in a substrate **202** such as a silicon wafer by an isolation structure such as a trench isolation structure **204** (**FIG. 2A**). Memory cells are to be formed in the first region, and logic devices are to be formed in the second region. In a step **104**, a tunnel oxide layer **210** is formed over the first and second regions **206**, **208** (**FIG. 2B**). In a step **104**, a layer of silicon nitride **212** is deposited over the tunnel oxide layer **210** (**FIG. 2C**). In a step **108**, the layer of silicon nitride is oxidized to form a top oxide layer **214**, consuming an upper portion of the silicon nitride layer and resulting in a silicon nitride layer **213** of reduced thickness (**FIG. 2D**). This completes formation of the ONO film. In a step **110**, masking and patterning processes are carried out to define ONO structures **220**, **222** over the first region **206** of the substrate **202**, exposing the surface of substrate **202** in the region **208**. Each resulting ONO structure **220**, **222** constitutes an ONO stack including, from the substrate **202** upward, a bottom oxide **224**, a silicon nitride **226**, and a top oxide **228**. The ONO stacks are separated by a source/drain region **230**, and in a step **112** an implant is carried out to form a buried diffusion **232**, constituting a buried source/drain (**FIG. 2E**). Then, in a step **112** an oxidation is carried out, resulting in growth of a device gate oxide **236** over the second region **208**, and in growth of a source/drain oxide **234**, consuming a portion of the buried diffusion and resulting in a buried diffusion **233** of reduced thickness (**FIG. 2F**). Under the conditions employed here, the thickness of the top oxide of the ONO structures increases only by a very small and relatively insignificant amount, typically a few A. In a step **116**, a polysilicon layer **238** is deposited over the gate oxide **236**, the ONO stacks **220**, **222**, and the buried source/drain oxide **234** (**FIG. 2G**).

[0036] As noted above, removal of the portion of the oxide layer **210** that overlies the second region **208** makes the overall process more complicated, and can result in an uneven substrate surface over the second region.

[0037] **FIG. 3** is a flow diagram of a process for oxide formation according to the invention. Resulting structures at various stages in the process **300** according to the invention are shown in diagrammatic sectional views in **FIGS. 4A through 4G**. In a step **302** of a process **300** according to the invention, a first region **406**, in which memory cells are to be formed, and a second region **408**, in which logic devices are to be formed, are defined in a substrate **402** such as a silicon wafer by an isolation structure such as a trench isolation structure **404** (**FIG. 4A**). In a step **304**, a tunnel oxide layer **410** is formed over the first and second regions **406**, **408** (**FIG. 4B**), and in a step **304**, a layer of silicon nitride **412** is deposited over the tunnel oxide layer **410** (**FIG. 4C**). These steps can be carried out using conven-

tional techniques and, as reference to **FIG. 4C** shows, these steps result in providing a substrate having regions defined by an isolation structure, and covered with a tunnel oxide layer which is overlain by a silicon nitride layer having an exposed surface. According to the invention, in a step **308** masking and patterning processes are carried out to define as shown at **420**, **422** the bottom oxide portion **424** and the silicon nitride portion **426** of the ONO structures to be completed over the first region **406** of the substrate **402**, exposing the surface of substrate **402** in the region **408** (**FIG. 4D**). At this point neither the gate oxide for the logic devices in the region **408**, nor the top oxide for the ONO structures, has yet been formed. The defined oxide and nitride portions of the respective partially completed ONO stacks are separated by a source/drain region **430**, and in a step **310** an implant is carried out to form a buried diffusion, constituting a buried source/drain **432** (**FIG. 4E**).

[**0038**] Then, according to the invention, in a step **312** a rapid thermal oxidation ("RTO") is carried out in the presence of an oxygen radical to form simultaneously a top oxide layer **428**, a buried drain/source oxide layer **434**, and a gate oxide layer **436** (**FIG. 4F**). As the top oxide layer **428** is grown, a portion of the silicon nitride layer **426** is consumed, leaving a thinner silicon nitride layer **427**. Each resulting ONO structure **421**, **423** constitutes an ONO stack including, from the substrate **402** upward, a bottom oxide **424**, a silicon nitride **427**, and a top oxide **428**.

[**0039**] Then, in a step **314** a polysilicon layer **438** is deposited over the gate oxide **436**, the ONO stacks **421**, **423**, and the buried source/drain oxide **434** (**FIG. 2G**).

[**0040**] Referring now to **FIG. 5**, there is shown in a diagrammatic sectional view an ONO structure **500** formed in a memory cell region according to a conventional process. The ONO structure **500** is formed on a substrate **502**, and includes an ONO stack **522**, made up of, from the substrate upward, a bottom oxide **524**, a silicon nitride **526** and a top oxide **528**. Buried diffusions (source/drain regions) **532** have been formed by implant into the substrate adjacent the ONO stack, and source/drain oxides **534** have been grown from the buried diffusions **532**. The top oxide of the ONO structure and the adjacent source/drain oxides are covered by a polysilicon layer **538**. As noted above, the formation of a top oxide in the ONO structure using a conventional wet oxidation is followed by a cleaning process, which can etch the top oxide layer and expose the corners or edges of the silicon nitride layer. Referring again to **FIG. 5**, in an ONO stack formed in the conventional way the edges **527** of the silicon nitride layer, which were exposed as a result of etching the edges **529** of the top oxide layer **528**. When the polysilicon **538** is deposited over the stack, the exposed edges **527** of the nitride contact the overlying polysilicon **538**, providing a route for charge leakage from the nitride into the polysilicon, and degrading the performance of the ONO structure.

[**0041**] This problem is avoided according to the invention, as **FIG. 6** shows in a diagrammatic sectional view of an ONO structure **600** formed according to the invention. The ONO structure **600** according to the invention is formed on a substrate **602**, and includes an ONO stack **622**, made up of, from the substrate upward, a bottom oxide **624**, a silicon nitride **626** and a top oxide **628**. Buried diffusions (source/drain regions) **632** have been formed by implant into the substrate adjacent the ONO stack, and source/drain oxides **634** have been grown from the buried diffusions **632** during the oxide radical-containing RTO at the same time as the top oxide **628** was formed, as described above with reference to **FIG. 3** and **FIG. 4D-4F**. The top oxide of the ONO structure and the adjacent source/drain oxides are covered by a polysilicon layer **638**. According to the invention, the top oxide is grown from exposed surfaces of the silicon nitride layer following patterning of the nitride and bottom oxide portions, and as a result the corners, or edges, of the silicon nitride layer as formed in this way are entirely covered by oxide, which wraps around the edges of the silicon nitride layer to contact the adjacent portions of the drain/source oxide. As a result the nitride is entirely isolated from the subsequently-formed overlying polysilicon layer, providing an ONO structure having improved performance and reliability.

EXAMPLES

Example 1

[**0042**] In this example, patterned Si and SiN surfaces were formed on a wafer substrate, and the wafer was placed in an in situ steam generation furnace. The wafer was heated to about 950° C. in the ISSG chamber, and was exposed to H_2 at 2 slm and O_2 at 8 slm in N_2 as a carrier gas for about 300 seconds, to form oxides on Si to a thickness about 158 Å and SiN to a thickness about 128 Å.

Example 2

[**0043**] In this example, a practical rate of oxide growth on silicon nitride using an ISSG process is compared with a theoretical rate derived from reaction equations.

[**0044**] The theoretical rate can be derived as follows:

$$Si_3N_{4+6}H_2O \rightarrow 3SiO_{2+4}NH_3$$

Si_3N_4:(28.086·3+14·4 *g*/mole)/(3.1 *g*/*cm*^{2})=45.25 *cm*^{3}/mole

SiO_2:(28+16·2 *g*/mole)/(2.21 *g*/*cm*^{2})=27.18 *cm*^{3}/mole

(27.18·3)/45.25=1.8

[**0045**] A plot of experimental data for oxide growth thickness on (SiNGen) silicon nitride versus silicon nitride consumed thickness using an ISSG process yielded a slope of 1.6301. The difference between the theoretical rate and the measured experimental rate may be accounted for by formation of nitrogen-incorporated oxide (oxynitride) in a thin layer at the interface between the top oxide and the nitride, making a precise location of the oxide—nitride interface difficult to determine, particularly in the thin top oxide film of the ONO stack.

Example 3

[**0046**] In this example the oxide growth rate on (DCS) silicon nitride was compared with that on a silicon substrate using an ISSG process at three temperatures: 850° C., 900° C., and 950° C. Wafers at each temperature were exposed to hydrogen and oxygen flowed at a ratio (H_2/H_2+O_2) about 33% (H_2 at 6 slm and O_2 at 12 slm), and oxide thicknesses

were measured at time intervals of about 30 seconds, 60 seconds, 90 seconds, and 120 seconds.

[0047] In the 850° C. process, the ratio of growth rates on silicon nitride and on silicon (SiN/Si) ranged about 0.68:1 to 0.75:1; in the 900° C. process, the ratio of growth rates on silicon nitride and on silicon (SiN/Si) ranged about 0.69:1 to 0.75:1; and in the 950° C. process, the ratio of growth rates on silicon nitride and on silicon (SiN/Si) ranged about 0.72:1 to 0.78:1.

[0048] Formation of thin oxide films on nitride using conventional methods follows a linear growth law. In contrast, formation of oxide by ISSG is apparently diffusion controlled, as the square of oxide thickness values is linearly proportional to oxidation time, and it conforms to the parabolic growth law.

Example 4

[0049] In this example the oxide growth rate using an ISSG process on (DCS) silicon nitride was compared at two different hydrogen and oxygen ratios (H_2/H_2+O_2): about 25% and about 33%, at three temperatures: 850° C., 900° C., and 950° C.; and oxide thicknesses were measured at time intervals of about 30 seconds, 60 seconds, 90 seconds, and 120 seconds. The silicon nitride films were prepared using a XT (lamp type) single wafer chamber. Generally, resulting oxides grown at the higher process temperatures were thicker at each time interval, that is, the oxide formation rate was higher at the higher temperatures. Apparently increased kinetic energy of the oxygen radicals enables them to overcome the activation barrier more readily. Also, at each process temperature the oxide formation rate was higher for the higher H_2/H_2+O_2 ratio. That is, for a given process temperature the process time to reach a specified oxide thickness is less at the higher hydrogen concentration. Apparently the higher concentration of hydrogen accelerates the dissociation of molecular oxygen to the reactive oxygen radicals and thereby makes more oxygen radicals available for reaction.

Example 5

[0050] In this example oxide was grown by ISSG at 850° C. and 950° C. on nitrides formed by a variety of methods, including DCS-based nitrides (XT lamp type chamber), silane-based nitrides grown by (XT lamp type) single wafer chambers, and silane-based nitrides grown using SiNGen single wafer chamber systems. As expected, top oxide growth rates were higher at the higher temperature. At each of the two temperatures growth rates were substantially similar on all three film types.

[0051] As will be appreciated from the foregoing, suitable values for one or more of the parameters will differ according to the values of one or more other parameters. Generally, for instance, the processing time can be reduced at higher processing temperatures. And, for instance, for any given processing temperature the processing time can be less at higher proportions of H_2 to O_2 in the gas mixture. The illustrative examples provided here suggest guidelines for determining, without undue experimentation, preferred combinations of parameters according to the invention other than the specific ones shown.

[0052] Other embodiments are within the following claims.

1. A method for forming an ONO structure, comprising:

providing an oxide-nitride film on a surface of a substrate, the oxide-nitride film including a first oxide layer over the substrate and a silicon nitride layer over the first oxide layer;

patterning the oxide-nitride film to define bottom oxide and silicon nitride portions of an ONO stack on the substrate, the bottom oxide and silicon nitride portions having exposed sidewalls and the silicon nitride portion having an exposed surface; and

exposing the exposed sidewalls and the exposed surface to a rapid thermal oxidation in an ambient containing a radical oxidizing agent, to form an oxide layer on the exposed surface and sidewalls of the patterned silicon nitride portion and on the sidewalls of the patterned bottom oxide portion.

2. The method of claim 1 wherein the radical oxidizing agent comprises an oxygen radical.

3. The method of claim 1 wherein the radical oxidizing agent comprises O.

4. The method of claim 1 wherein the exposing comprises heating the substrate to a selected temperature and exposing the exposed sidewalls and the exposed surface to a mixture of an oxygen-containing gas and a hydrogen-containing gas in a selected proportion at a selected pressure and for a selected time, whereby components of the oxygen-containing gas and the hydrogen-containing gas react to produce the radical oxidizing agent near the heated substrate.

5. The method of claim 4 wherein heating the substrate comprises heating the substrate to a temperature in a range about 700° C. to about 1300° C.

6. The method of claim 4 wherein heating the substrate comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

7. The method of claim 4 wherein heating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

8. The method of claim 1 wherein the exposing comprises heating the substrate to a selected temperature and exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the O_2 and H_2 react to produce O. near the heated substrate.

9. The method of claim 8 wherein the exposing comprises heating the substrate to a temperature in a range about 700° C. to about 1300° C., exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a proportion in a range about 0.1% to about 40% (H_2/H_2+O_2) at a pressure in a range about 1 torr to about 20 torr for a time in a range about 1 to 1000 seconds.

10. The method of claim 9 wherein the heating comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

11. The method of claim 9 wherein heating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

12. The method of claim 9 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 5% to about 33% (H_2/H_2+O_2).

13. The method of claim 9 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 1:19 to about 1:2 (H_2:O_2).

14. The method of claim 9 wherein the exposing comprises flowing the mixture of O_2 and H_2 over the heated substrate for a time in a range about 10 seconds to about 500 seconds.

15. The method of claim 9 wherein the exposing comprises flowing the mixture of O_2 and H_2 over the heated substrate for a time in a range about 30 seconds to about 300 seconds.

16. The method of claim 1 wherein the exposing comprises heating the substrate in a furnace and flowing into the furnace a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the O_2 and H_2 react to produce O. near the heated substrate.

17. The method of claim 16 wherein flowing the mixture of O_2 and $1H_2$ further comprises flowing a carrier gas.

18. The method of claim 17 wherein flowing the mixture of O_2 and H_2 further comprises flowing N_2 as a carrier gas.

19. The method of claim 16 wherein flowing the mixture of O_2 and Hf_2 in a selected proportion comprises flowing the O_2 and H_2 at selected proportional flow rates.

20. The method of claim 19 wherein flowing the mixture of O_2 and H_2 further comprises flowing N_2 as a carrier gas at a selected flow rate.

21. The method of claim 19 wherein flowing the O_2 and H_2 comprises flowing O_2 and H_2 at a combined flow rate in a range about 1 to about 40 slm.

22. The method of claim 20 wherein flowing the O_2 and H_2 comprises flowing O_2 and H_2 at a combined flow rate in a range about 1 to about 40 slm, and flowing N_2 comprises flowing N_2 at a flow rate up to about 50 shm.

23. A method for manufacturing a semiconductor device having an ONO structure, comprising:

providing an oxide-nitride film on a surface of a substrate, the substrate having first and second regions defined by an isolation, the oxide-nitride film including a first silicon oxide layer over the substrate and a silicon nitride layer over the first silicon oxide layer;

patterning the oxide-nitride film to expose a surface of the substrate in the second region and to define bottom oxide and silicon nitride portions of an ONO stack in the first region of the substrate, the bottom oxide portion and silicon nitride portions having exposed sidewalls and the silicon nitride portion having an exposed surface; and

exposing the exposed sidewalls and the exposed surface to a radical oxidizing agent while the substrate is at a temperature in a range about 700° C. to about 1200° C., to form concurrently a second oxide layer on the exposed surface and sidewails of the patterned silicon nitride portion and a gate oxide layer on the substrate surface in the second region; and

forming a conductive layer over the second oxide layer and over the gate oxide layer.

24. The method of claim 23 wherein the radical oxidizing agent comprises an oxygen radical.

25. The method of claim 23 wherein the radical oxidizing agent comprises O.

26. The method of claim 23 wherein the exposing comprises heating the substrate to the temperature in the temperature range and exposing the exposed sidewalls and the exposed surface to a mixture of an oxygen-containing gas and a hydrogen-containing gas in a selected proportion at a selected pressure and for a selected time, whereby components of the oxygen-containing gas and the hydrogen-containing gas react to produce the radical oxidizing agent near the heated substrate.

27. The method of claim 26 wherein heating the substrate comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

28. The method of claim 26 wherein beating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

29. The method of claim 23 wherein the exposing comprises heating the substrate to the temperature in the temperature range and exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the O_2 and H_2 react to produce O. near the heated substrate.

30. The method of claim 29 wherein the exposing comprises heating the substrate to a temperature in temperature range, exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a proportion in a range about 0.1% to about 40% (H_2/H_2+O_2) at a pressure in a range about 1 torr to about 20 torr for a time in a range about 1 to 1000 seconds.

31. The method of claim 30 wherein the heating comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

32. The method of claim 30 wherein heating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

33. The method of claim 30 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 5% to about 33% (H_2/H_2+O_2).

34. The method of claim 30 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 1:19 to about 1:2 (H_2:O_2).

35. The method of claim 30 wherein the exposing comprises flowing the mixture of O_2 and H_2 over the heated substrate for a time in a range about 10 seconds to about 500 seconds.

36. The method of claim 30 wherein the exposing comprises flowing the mixture of O_2 and Hz over the heated substrate for a time in a range about 30 seconds to about 300 seconds.

37. The method of claim 23 wherein the exposing comprises heating the substrate in a furnace and flowing into the Face a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the O_2 and H_2 react to produce O. near the heated substrate.

38. The method of claim 37 wherein flowing the mixture of O_2 and H_2 further comprises flowing a carrier gas.

39. The method of claim 38 wherein flowing the mixture of O_2 and H_2 further comprises flowing N_2 as a carrier gas.

40. The method of claim 37 wherein flowing the mixture of O_2 and H_2 in a selected proportion comprises flowing the O_2 and H_2 at selected proportional flow rates.

41. The method of claim 40 wherein flowing the mixture of O_2 and H_2 further comprises flowing N_2 as a carrier gas at a selected flow rate.

42. The method of claim 40 wherein flowing the O_2 and H_2 comprises flowing O_2 and H_2 at a combined flow rate in a range about 1 to about 40 slm.

43. The method of claim 41 wherein flowing the O_2 and H_2 comprises flowing O_2 and H_2 at a combined flow rate in a range about 1 to about 40 slm, and flowing N_2 comprises flowing N_2 at a flow rate up to about 50 slm.

44. The method of claim 23 wherein a ratio of thicknesses of the formed second oxide layer and the formed gate oxide layer is in a range about 0.6:1 to about 0.8:1.

45. The method of claim 23 wherein the exposing comprises heating the substrate in a furnace and generating the radical oxidizing agent within the furnace while holding the substrate at a temperature in the temperature range for a time in a range about 10 seconds to about 500 seconds.

46. The method of claim 23 wherein the exposing comprises heating the substrate in a furnace and generating the radical oxidizing agent within the furnace while holding the substrate at a temperature in the temperature range for a time in a range about 30 seconds to about 300 seconds.

47. A method for manufacturing a memory device having an ONO structure, comprising:

providing an oxide-nitride film on a surface of a substrate, the substrate having first and second regions defined by an isolation, the oxide-nitride film including a first silicon oxide layer over the substrate and a silicon nitride layer over the first silicon oxide layer,

patterning the oxide-nitride film to expose a surface of the substrate in the second region and to define bottom oxide and silicon nitride portions of an ONO stack in the first region of the substrate, the bottom oxide portion and silicon nitride portions having exposed sidewalls and the silicon nitride portion having an exposed surface; and

exposing the exposed sidewalls and the exposed surface to a radical oxidizing agent while the substrate is at a temperature in a range about 700° C. to about 1200° C., to form concurrently a second oxide layer on the exposed surface and sidewalls of the patterned silicon nitride portion and a gate oxide layer on the substrate surface in the second region; and

forming a conductive layer over the second oxide layer and over the gate oxide layer.

48. The method of claim 47 wherein the radical oxidizing agent comprises an oxygen radical.

49. The method of claim 47 wherein the radical oxidizing agent comprises O.

50. The method of claim 47 wherein the exposing comprises heating the substrate to the temperature in the temperature range and exposing the exposed sidewalls and the exposed surface to a mixture of an oxygen-containing gas and a hydrogen-containing gas in a selected proportion at a selected pressure and for a selected time, whereby components of the oxygen-containing gas and the hydrogen-containing gas react to produce the radical oxidizing agent near the heated substrate.

51. The method of claim 50 wherein heating the substrate comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

52. The method of claim 50 wherein heating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

53. The method of claim 47 wherein the exposing comprises heating the substrate to the temperature in the temperature range and exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the O_2 and H_2 react to produce O. near the heated substrate.

54. The method of claim 53 wherein the exposing comprises heating the substrate to a temperature in temperature range, exposing the exposed sidewalls and the exposed surface to a mixture of O_2 and H_2 in a proportion in a range about 0.1% to about 40% (H_2/H_2+O_2) at a pressure in a range about 1 torr to about 20 torr for a time in a range about 1 to 1000 seconds.

55. The method of claim 54 wherein the heating comprises heating the substrate to a temperature in a range about 900° C. to about 1150° C.

56. The method of claim 54 wherein heating the substrate comprises heating the substrate to a temperature in a range about 850° C. to about 1000° C.

57. The method of claim 54 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 5% to about 33% (H_2/H_2+O_2).

58. The method of claim 54 wherein the exposing comprises flowing over the heated substrate a mixture of O_2 and H_2 in a proportion in a range about 1:19 to about 1:2 (H_2:O_2).

59. The method of claim 54 wherein the exposing comprises flowing the mixture of O_2 and H_2 over the heated substrate for a time in a range about 10 seconds to about 500 seconds.

60. The method of claim 54 wherein the exposing comprises flowing the mixture of O_2 and H_2 over the heated substrate for a time in a range about 30 seconds to about 300 seconds.

61. The method of claim 47 wherein the exposing comprises heating the substrate in a furnace and flowing into the furnace a mixture of O_2 and H_2 in a selected proportion at a selected pressure and for a selected time, whereby components of the 2 and 12 react to produce O near the heated substrate.

62. The method of claim 61 wherein flowing the mixture of O_2 and H_2 further comprises flowing a carrier gas.

63. The method of claim 62 wherein flowing the mixture of O_2 and H_2 further comprises flowing N_2 as a carrier gas.

64. The method of claim 61 wherein flowing the mixture of O_2 and H_2 in a selected proportion comprises flowing the O_2 and H_2 at selected proportional flow rates.

65. The method of claim 64 wherein flowing the mixture of O_2 and H_2 filer comprises flowing N_2 as a carrier gas at a selected flow rate.

66. The method of claim 64 wherein flowing the O_2 and H_2 comprises flowing O_2 and H_2 at a combined flow rate in a range about 1 to about 40 slm.

67. The method of claim 65 wherein flowing the O_2 and H_2 comprises flowing (n and H_2 at a combined flow rate in a range about 1 to about 40 shm, and flowing N_2 comprises flowing N_2 at a flow rate up to about 50 slm.

68. The method of claim 47 wherein a ratio of thicknesses of the formed second oxide layer and the formed gate oxide layer is in a range about 0.6:1 to about 0.8:1.

69. The method of claim 47 wherein the exposing comprises heating the substrate in a furnace and generating the radical oxidizing agent within the furnace while holding the substrate at a temperature in the temperature range for a time in a range about 10 seconds to about 500 seconds.

70. The method of claim 47 wherein the exposing comprises heating the substrate in a furnace and generating the radical oxidizing agent within the furnace while holding the substrate at a temperature in the temperature range for a time in a range about 30 seconds to about 300 seconds.

71. A semiconductor device having a silicon oxide/silicon nitride/silicon oxide structure, comprising

a first silicon oxide layer over a substrate;

a silicon nitride layer over a portion of the first silicon oxide layer;

a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer; and

a gate conducting layer over the silicon oxide layer.

72. A memory cell having a silicon oxide/silicon nitride/silicon oxide structure, comprising

a buried drain and a buried source within a substrate;

a buried drain oxide layer over the buried drain and a buried source oxide layer over the buried source;

a first silicon oxide layer covering a region of the substrate located between the buried drain and the buried source and covering a portion of the buried drain oxide layer and a portion of the buried source oxide layer;

a silicon nitride layer covering a portion of the first silicon oxide layer;

a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer;

and a gate conducting layer over the second silicon oxide layer.

73. A memory cell having a silicon oxide/silicon nitride/silicon oxide structure in a read-only memory, comprising:

a buried drain and a buried source located within a substrate;

a buried drain oxide layer over the buried drain and a buried source oxide layer over the buried source;

a first silicon oxide layer covering a region of the substrate located between the buried drain and the buried source and covering a portion of the buried drain oxide layer and a portion of the buried source oxide layer;

a silicon nitride layer covering a portion of the first silicon oxide layer;

a second silicon oxide layer fully covering the silicon nitride layer and contacting the first silicon oxide layer; and

a gate conducting layer over the second silicon oxide layer.

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